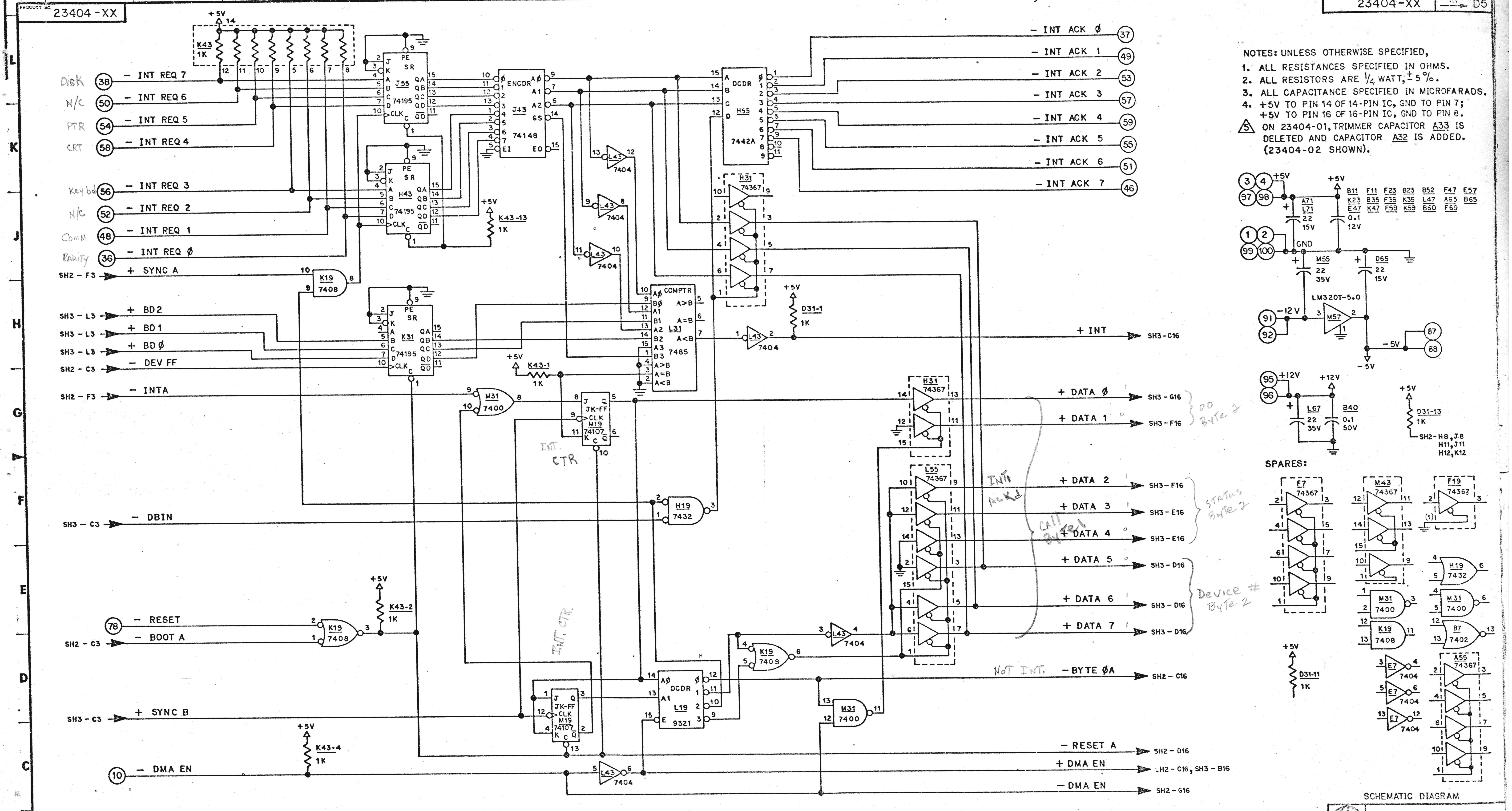
Diablo Systems Incorporated

Schematic Diagrams

Model________ Serial No.________

CS500-09 2/75

23404-XX



+5V
K43 1K
Disk (38) - INT REQ 7
N/C (50) - INT REQ 6
PTR (54) - INT REQ 5
CRT (58) - INT REQ 4
Keybd (56) - INT REQ 3
N/C (52) - INT REQ 2
Comm (48) - INT REQ 1
Parity (36) - INT REQ 0
SH2 - F3 + SYNC A
K19 7408
J55 74195
H43 74195
J43 74148 ENCDR
H55 7442A DCDR
L43 7404
K43-13 1K
H31 74367
(37) - INT ACK 0
(49) - INT ACK 1
(53) - INT ACK 2
(57) - INT ACK 3
(59) - INT ACK 4
(55) - INT ACK 5
(51) - INT ACK 6
(46) - INT ACK 7
SH3 - L3 + BD2
SH3 - L3 + BD1
SH3 - L3 + BD0
SH2 - C3 - DEV FF
K31 74195
L31 7485 COMPTR
D31-1 1K
+ INT SH3-C16
SH2 - F3 - INTA
M31 7400
K43-1 1K
M19 74107 JK-FF
INT. CTR
H31 74367
+ DATA 0 SH3-G16
+ DATA 1 SH3-F16
I/O Byte 1
L55 74367
INT Ack'd
+ DATA 2 SH3-F16
+ DATA 3 SH3-E16
+ DATA 4 SH3-E16
Status Byte 2
Call Byte 1
+ DATA 5 SH3-D16
+ DATA 6 SH3-D16
+ DATA 7 SH3-D16
Device # Byte 2
H19 7432
SH3 - C3 - DBIN
K43-2 1K
(78) - RESET
SH2 - C3 - BOOT A
K19 7408
INT. CTR.
L19 9321 DCDR
Not INT. - BYTE 0A SH2-C16
M31 7400
SH3 - C3 + SYNC B
M19 74107 JK-FF
K43-4 1K
(10) - DMA EN
- RESET A SH2-D16
+ DMA EN SH2-C16, SH3-B16
- DMA EN SH2-G16
(3)(4) +5V (97)(98)
+5V
B11 F11 F23 B23 B52 F47 E57
K23 B35 F35 K35 L47 A65 B65
E47 K47 F59 K59 B60 F69
A71 L71 22 15V
0.1 12V
(1)(2) (99)(100) GND
M55 22 35V
D65 22 15V
LM320T-5.0 M57
(91)(92) -12V
-5V (87)(88)
-5V
(95)(96) +12V
+12V
L67 22 35V
B40 0.1 50V
+5V
D31-13 1K
SH2-H8, J8 H11, J11 H12, K12
SPARES:
F7 74367
M43 74367
F19 74367
H19 7432
M31 7400
M31 7400
K19 7408
B7 7402
E7 7404
A55 74367
+5V
D31-11 1K

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. ON 23404-01, TRIMMER CAPACITOR A33 IS DELETED AND CAPACITOR A32 IS ADDED. (23404-02 SHOWN).

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

PW ASSY, PROC 2

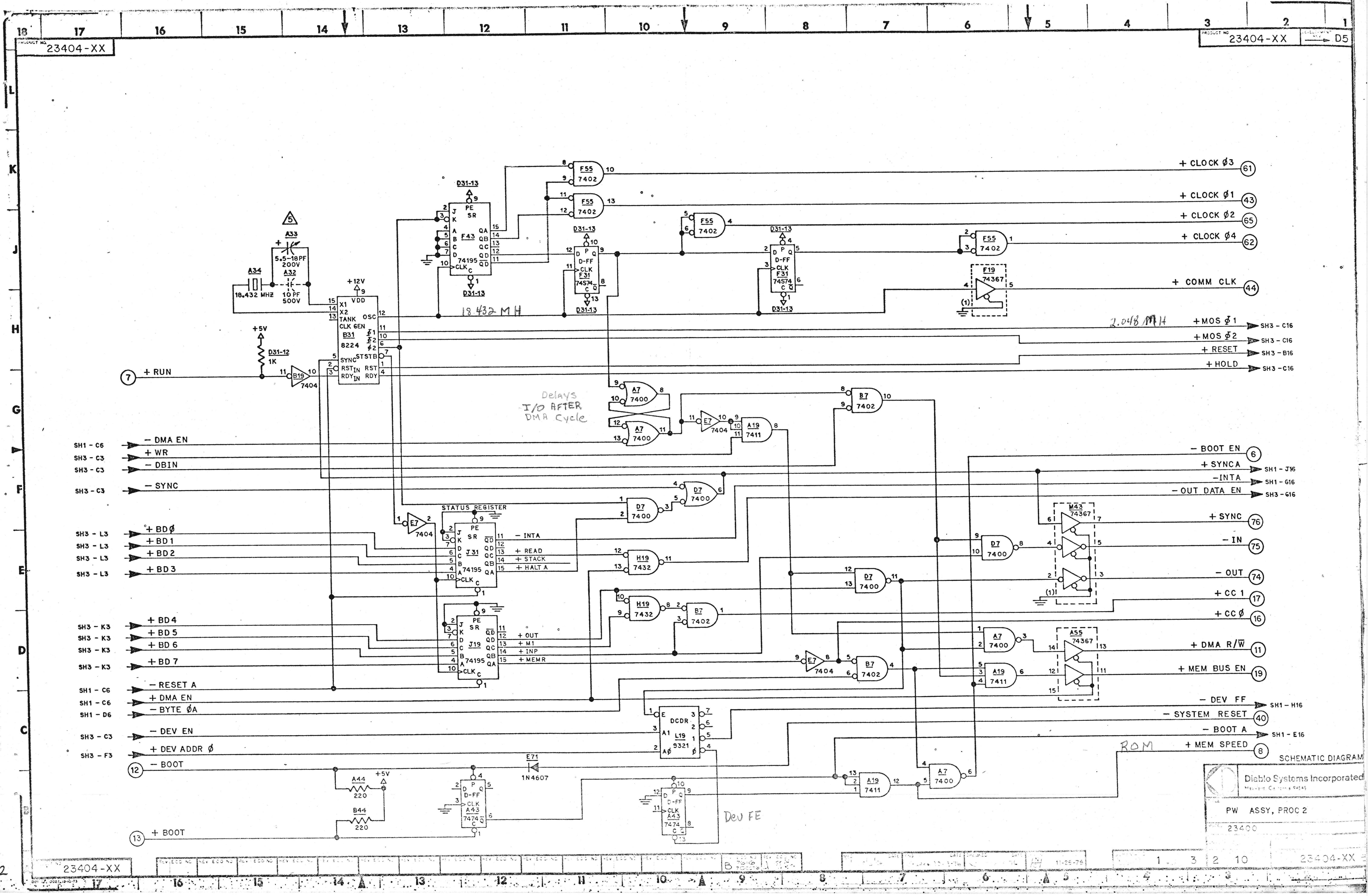
MODEL 23400

12-17-75

1 THRU 3

1 10

23404-XX


23404-XX
D5
+ CLOCK Ø3 61
+ CLOCK Ø1 43
+ CLOCK Ø2 65
+ CLOCK Ø4 62
+ COMM CLK 44
F55 7402
F43 74195
D31-13
F31 74S74
D-FF
F19 74367
A33 5.5-18PF 200V
A32 10 PF 500V
A34 18.432 MHZ
B31 8224
+12V
+5V
D31-12 1K
18.432 MH
2.048 MH
+MOS Ø1 SH3 - C16
+MOS Ø2 SH3 - C16
+ RESET SH3 - B16
+ HOLD SH3 - C16
7 + RUN
B19 7404
Delays I/O AFTER DMA Cycle
A7 7400
E7 7404
A19 7411
B7 7402
SH1 - C6 − DMA EN
SH3 - C3 + WR
SH3 - C3 − DBIN
SH3 - C3 − SYNC
− BOOT EN 6
+ SYNCA SH1 - J16
−INTA SH1 - G16
− OUT DATA EN SH3 - G16
D7 7400
STATUS REGISTER
J31 74195
− INTA
+ READ
+ STACK
+ HALT A
SH3 - L3 + BDØ
SH3 - L3 + BD1
SH3 - L3 + BD2
SH3 - L3 + BD3
H19 7432
M43 74367
+ SYNC 76
− IN 75
− OUT 74
+ CC 1 17
+ CC Ø 16
SH3 - K3 + BD4
SH3 - K3 + BD5
SH3 - K3 + BD6
SH3 - K3 + BD7
J19 74195
+ OUT
+ M1
+ INP
+ MEMR
A55 74367
+ DMA R/W̄ 11
+ MEM BUS EN 19
SH1 - C6 − RESET A
SH1 - C6 + DMA EN
SH1 - D6 − BYTE ØA
SH3 - C3 − DEV EN
SH3 - F3 + DEV ADDR Ø
DCDR L19 9321
− DEV FF SH1 - H16
− SYSTEM RESET 40
− BOOT A SH1 - E16
+ MEM SPEED 8
ROM
12 − BOOT
E71 1N4607
A44 220
B44 220
A43 7474
Dev FE
13 + BOOT

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

Hayward, California 94545

PW ASSY, PROC 2

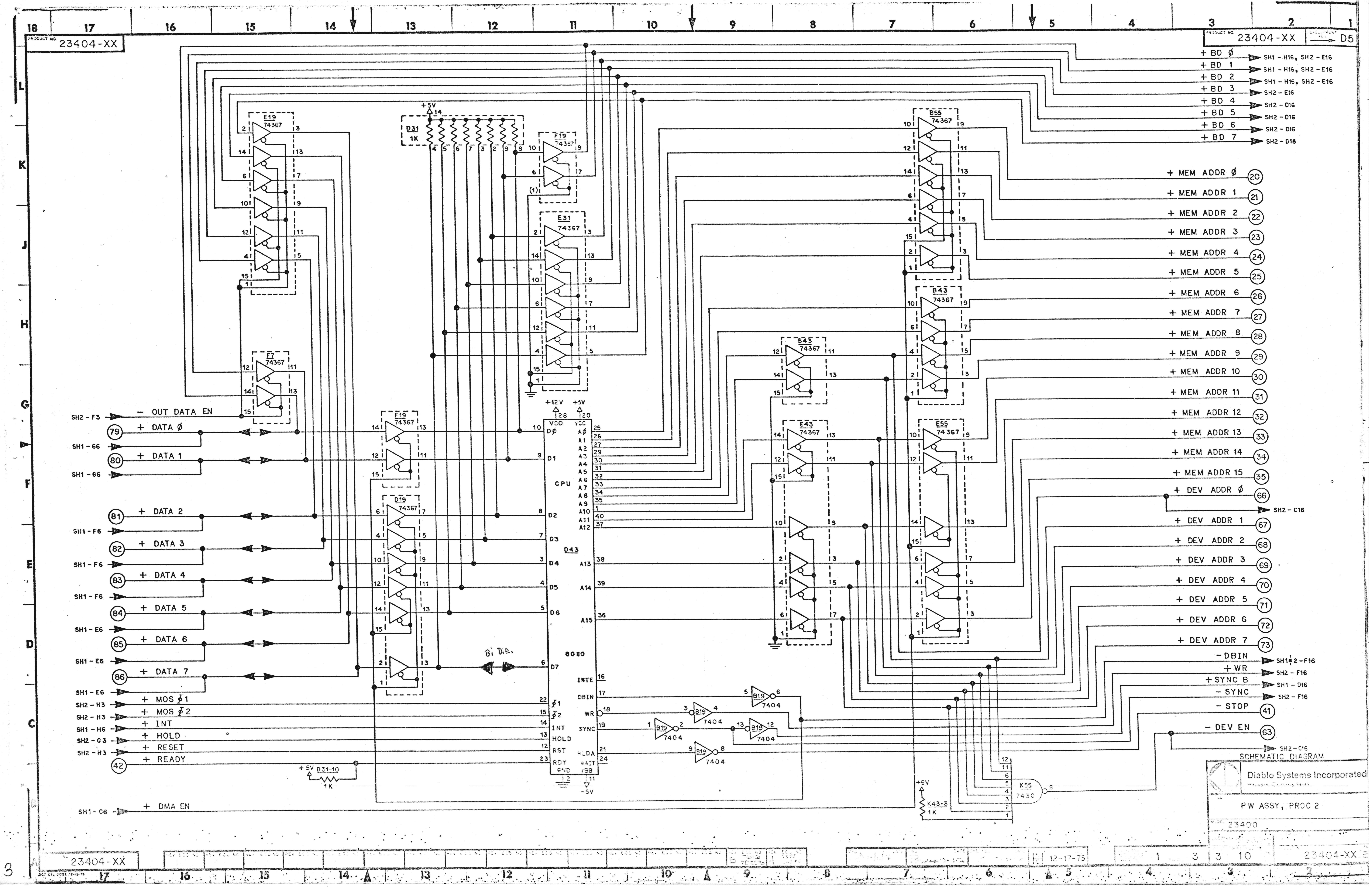
23400

1 3 2 10

23404-XX

11-26-75

2



23404-XX
D5
+ BD 0
+ BD 1
+ BD 2
+ BD 3
+ BD 4
+ BD 5
+ BD 6
+ BD 7
SH1 - H16, SH2 - E16
SH2 - E16
SH2 - D16
+ MEM ADDR 0
+ MEM ADDR 1
+ MEM ADDR 2
+ MEM ADDR 3
+ MEM ADDR 4
+ MEM ADDR 5
+ MEM ADDR 6
+ MEM ADDR 7
+ MEM ADDR 8
+ MEM ADDR 9
+ MEM ADDR 10
+ MEM ADDR 11
+ MEM ADDR 12
+ MEM ADDR 13
+ MEM ADDR 14
+ MEM ADDR 15
+ DEV ADDR 0
SH2 - C16
+ DEV ADDR 1
+ DEV ADDR 2
+ DEV ADDR 3
+ DEV ADDR 4
+ DEV ADDR 5
+ DEV ADDR 6
+ DEV ADDR 7
- DBIN
SH1&2 - F16
+ WR
SH2 - F16
+ SYNC B
SH1 - D16
- SYNC
SH2 - F16
- STOP
- DEV EN
SH2 - C16
E19 74367
F19 74367
D31 1K
+5V
E31 74367
F7 74367
B55 74367
B43 74367
E43 74367
E55 74367
D19 74367
D43
CPU
8080
+12V
+5V
VDD
VCC
D0 D1 D2 D3 D4 D5 D6 D7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
INTE
DBIN
WR
SYNC
HLDA
WAIT
GND
-5V
Bi Dir.
SH2 - F3
- OUT DATA EN
+ DATA 0
+ DATA 1
+ DATA 2
+ DATA 3
+ DATA 4
+ DATA 5
+ DATA 6
+ DATA 7
SH1 - G6
SH1 - F6
SH1 - E6
+ MOS Φ1
+ MOS Φ2
+ INT
+ HOLD
+ RESET
+ READY
SH2 - H3
SH1 - H6
SH2 - G3
Φ1
Φ2
INT
HOLD
RST
RDY
+5V D31-10 1K
B19 7404
K55 7430
K43-3 1K
+ DMA EN
SH1 - C6

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

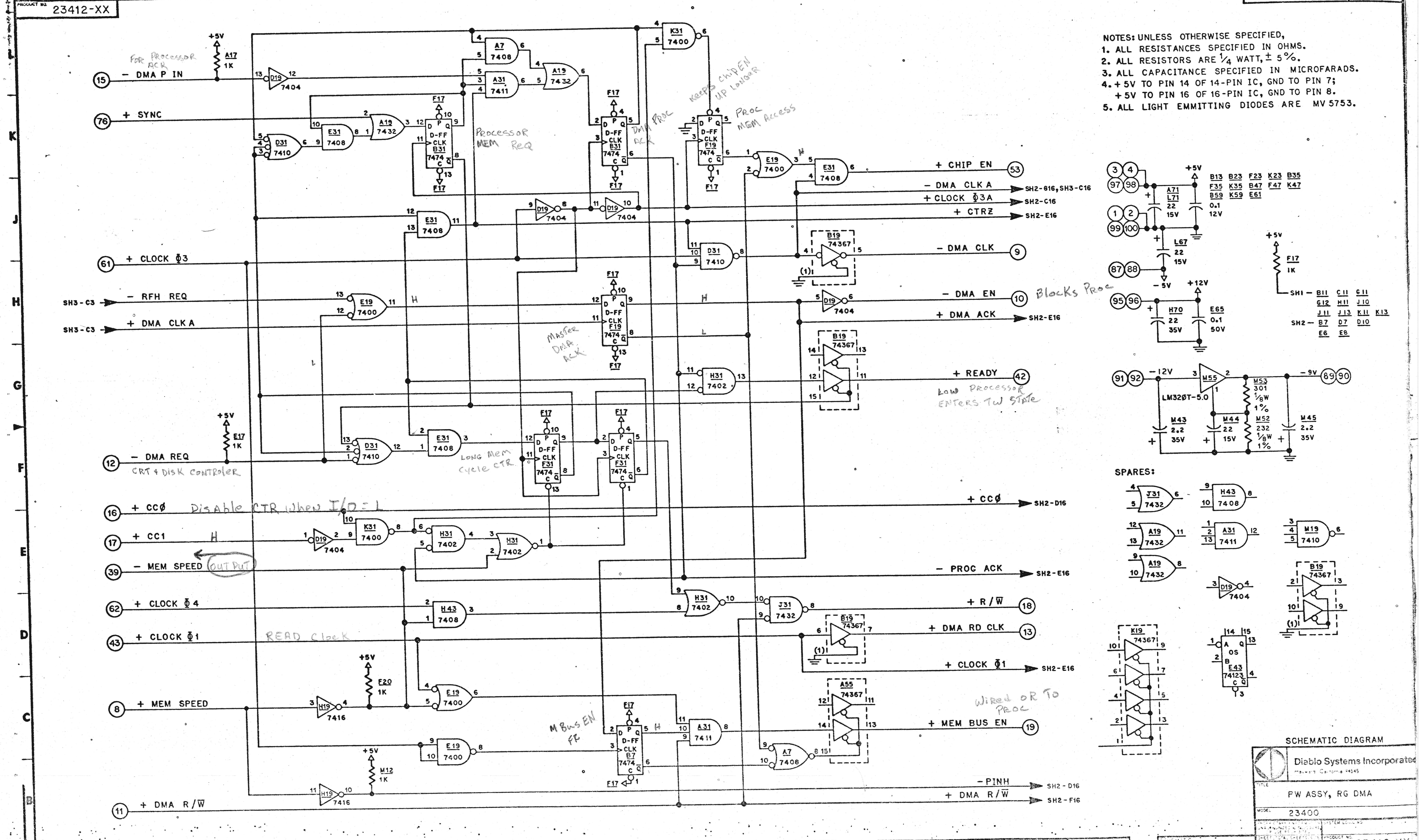
PW ASSY, PROC 2

23400

12-17-75

1 3 3 10

23404-XX



15 − DMA P IN
FOR PROCESSOR ACK
+5V
A17 1K
D19 7404
76 + SYNC
A19 7432
E31 7408
D31 7410
B31 7474 D-FF
F17
PROCESSOR MEM REQ
A7 7408
A31 7411
K31 7400
DMA PROC ACK
Keeps CHIP EN UP LONGER
F19 7474
Proc MEM Access
E19 7400
+ CHIP EN 53
− DMA CLK A SH2-E16, SH3-C16
+ CLOCK Φ3A SH2-C16
+ CTRZ SH2-E16
61 + CLOCK Φ3
B19 74367
− DMA CLK 9
SH3-C3 − RFH REQ
SH3-C3 + DMA CLK A
MASTER DMA ACK
− DMA EN 10 Blocks Proc
+ DMA ACK SH2-E16
H31 7402
+ READY 42
Low PROCESSOR ENTERS TW STATE
12 − DMA REQ CRT + DISK CONTROLER
F31 7474
LONG MEM CYCLE CTR
16 + CC0 Disable CTR When I/D = L
+ CC0 SH2-D16
17 + CC1
39 − MEM SPEED OUTPUT
− PROC ACK SH2-E16
62 + CLOCK Φ4
H43 7408
+ R/W̄ 18
J31 7432
43 + CLOCK Φ1 READ Clock
+ DMA RD CLK 13
+ CLOCK Φ1 SH2-E16
8 + MEM SPEED
H19 7416
F20 1K
M Bus EN FF
B7 7474
A55 74367
+ MEM BUS EN 19
Wired OR To Proc
M12 1K
− PINH SH2-D16
11 + DMA R/W̄
+ DMA R/W̄ SH2-F16
+5V
B13 B23 F23 K23 B35 F35 K35 B47 F47 K47 B59 K59 E61
A71 L71 22 15V 0.1 12V
L67 22 15V
−5V +12V
H70 22 35V
E65 0.1 50V
F17 1K
SH1 − B11 C11 G11 G12 H11 J10 J11 J13 K11 K13
SH2 − B7 D7 D10 E6 E8
−12V M55 LM320T-5.0 −9V
M53 301 1/8W 1%
M43 2.2 35V
M44 22 15V
M52 232 1/8W 1%
M45 2.2 35V
SPARES:
J31 7432
H43 7408
A19 7432
A31 7411
M19 7410
D19 7404
B19 74367
K19 74367
E43 74123 OS

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. + 5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
+ 5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. ALL LIGHT EMMITTING DIODES ARE MV 5753.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE PW ASSY, RG DMA

MODEL 23400

SCHEMATIC SHEETS 1 THRU 3

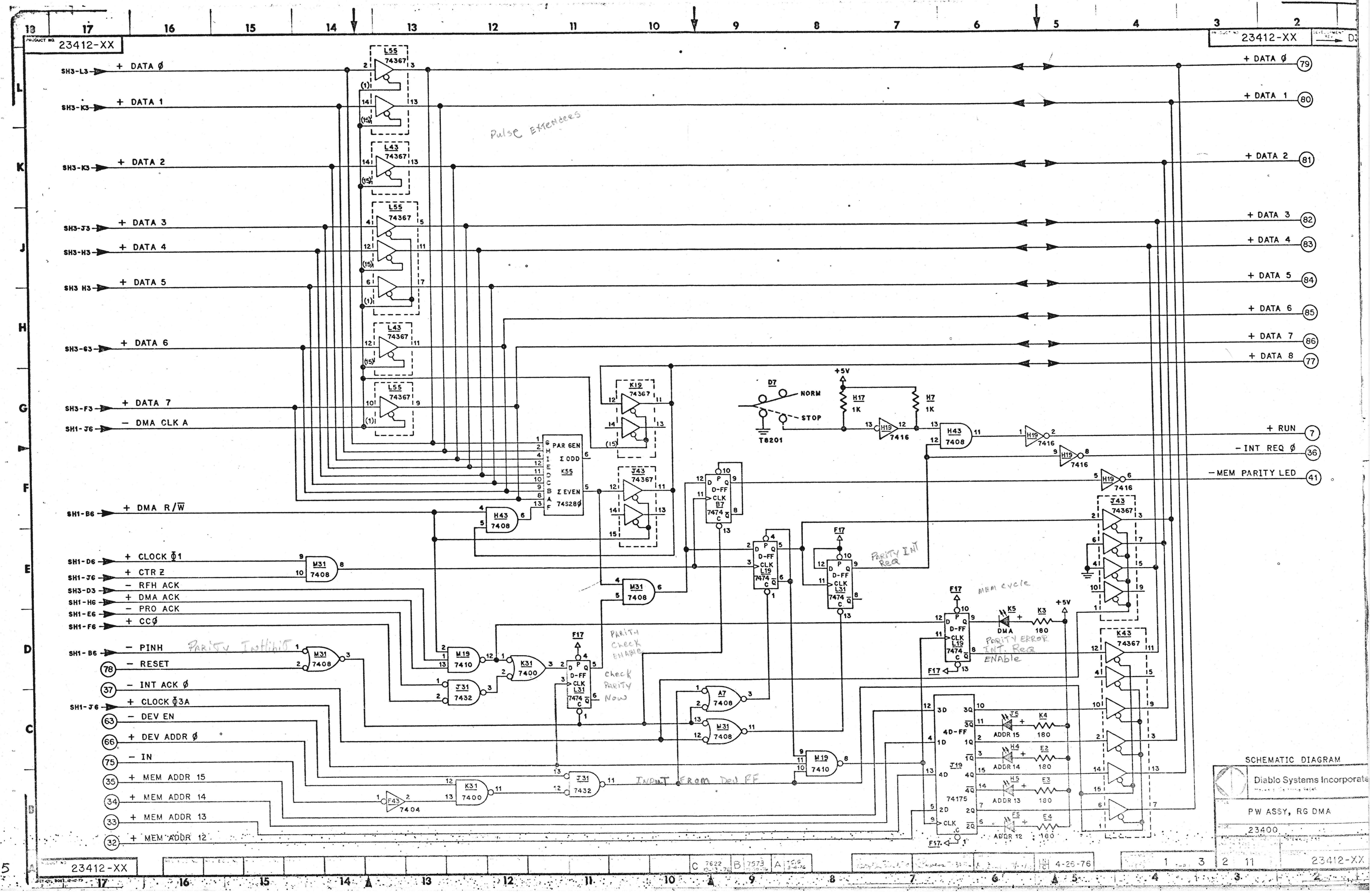
SHEET 1 TOTAL SHEETS 11 D

PRODUCT NO. 23412-XX

DEVELOPMENT REV D3

C 7E22 | B 7573 | A 759

4-21-76


23412-XX
+ DATA 0
+ DATA 1
+ DATA 2
+ DATA 3
+ DATA 4
+ DATA 5
+ DATA 6
+ DATA 7
+ DATA 8
SH3-L3
SH3-K3
SH3-J3
SH3-H3
SH3-G3
SH3-F3
SH1-J6
SH1-B6
SH1-D6
SH3-D3
SH1-H6
SH1-E6
SH1-F6
- DMA CLK A
+ DMA R/W̄
+ CLOCK Φ1
+ CTR Z
- RFH ACK
+ DMA ACK
- PRO ACK
+ CC0
- PINH
- RESET
- INT ACK 0
+ CLOCK Φ3A
- DEV EN
+ DEV ADDR 0
- IN
+ MEM ADDR 15
+ MEM ADDR 14
+ MEM ADDR 13
+ MEM ADDR 12
+ RUN
- INT REQ 0
- MEM PARITY LED
L55 74367
L43 74367
K19 74367
J43 74367
K43 74367
PAR GEN
Σ ODD
Σ EVEN
K55 74S280
H43 7408
M31 7408
M19 7410
J31 7432
K31 7400
F43 7404
A7 7408
B7 7474
L19 7474
L31 7474
J19 74175
H19 7416
D7
NORM
STOP
T8201
+5V
H17 1K
H7 1K
F17
K5 DMA
K3 180
J5 ADDR 15
K4 180
H4 ADDR 14
E2 180
H5 ADDR 13
E3 180
F5 ADDR 12
E4 180
4D-FF
D-FF
Pulse Extenders
Parity Inhibit
Parity Check Enable
Check Parity Now
Input From Dev FF
Parity Int Req
Mem cycle
Parity Error Int. Req Enable
79
80
81
82
83
84
85
86
77
7
36
41
78
37
63
66
75
35
34
33
32

SCHEMATIC DIAGRAM

Diablo Systems Incorporate

PW ASSY, RG DMA

23400

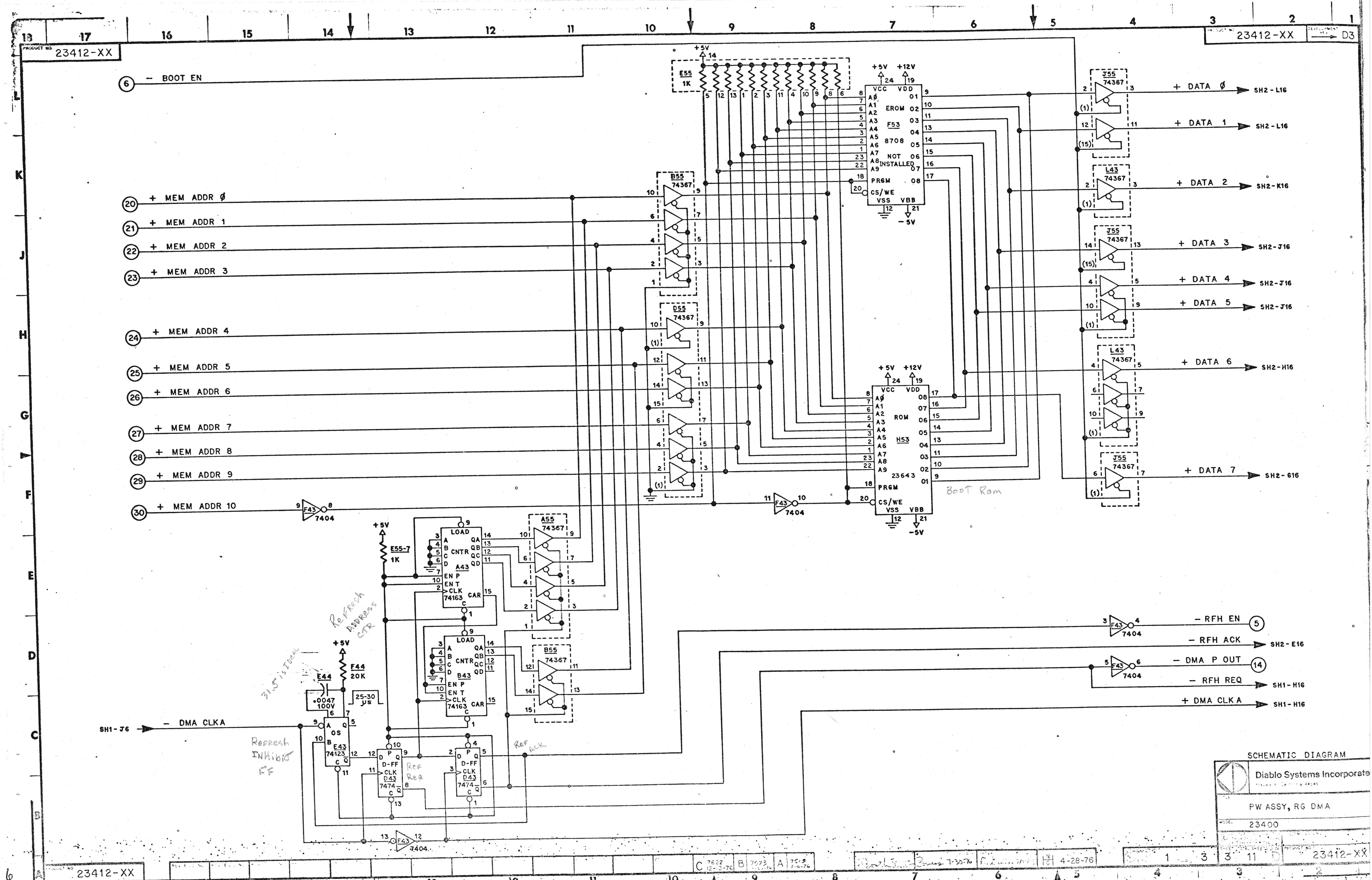
1 THRU 3

2 11

23412-XX

C 7622 | B 7573 | A

4-26-76


23412-XX
D3
6 − BOOT EN
20 + MEM ADDR 0
21 + MEM ADDR 1
22 + MEM ADDR 2
23 + MEM ADDR 3
24 + MEM ADDR 4
25 + MEM ADDR 5
26 + MEM ADDR 6
27 + MEM ADDR 7
28 + MEM ADDR 8
29 + MEM ADDR 9
30 + MEM ADDR 10
E55 1K
+5V
B55 74367
D55 74367
A55 74367
J55 74367
L43 74367
EROM F53 8708 NOT INSTALLED
ROM H53 23643
Boot Rom
VCC VDD
PRGM
CS/WE
VSS VBB
−5V
+12V
+ DATA 0 SH2-L16
+ DATA 1 SH2-L16
+ DATA 2 SH2-K16
+ DATA 3 SH2-J16
+ DATA 4 SH2-J16
+ DATA 5 SH2-J16
+ DATA 6 SH2-H16
+ DATA 7 SH2-G16
F43 7404
LOAD
CNTR
A43 74163
B43 74163
EN P
EN T
CLK
CAR
QA QB QC QD
E55-7 1K
Refresh Address CTR
F44 20K
E44 .0047 100V
25-30 µs
31.5 is ideal
E43 74123
OS
SH1-J6 − DMA CLKA
Refresh Inhibit FF
D-FF D43 7474
Ref Req
Ref Ack
− RFH EN 5
− RFH ACK SH2-E16
− DMA P OUT 14
− RFH REQ SH1-H16
+ DMA CLK A SH1-H16

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG DMA

MODEL 23400

C 7622 12-13-76 | B 7573 | A 7519 3-4-76

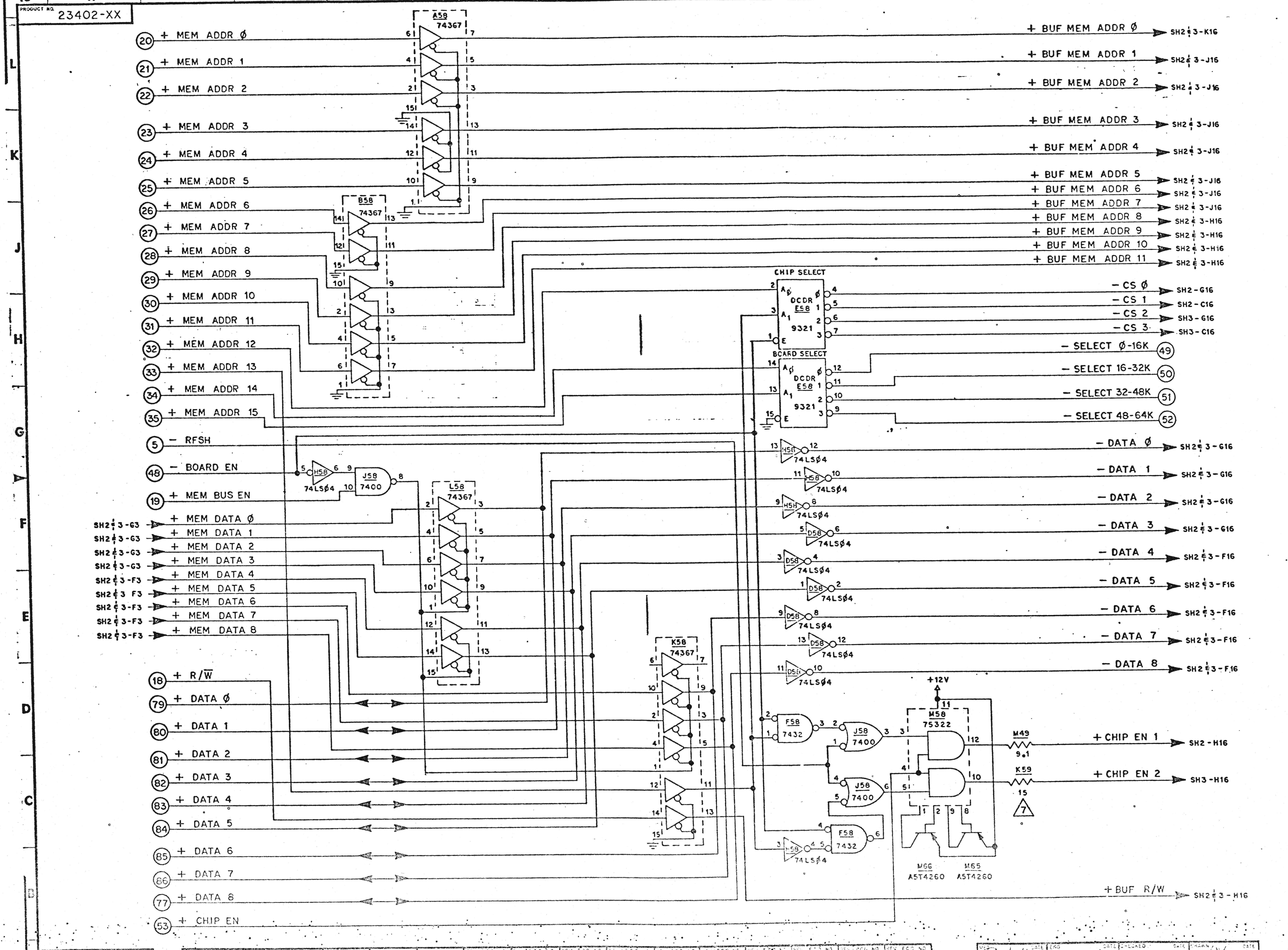
N/C 4-28-76

SHEET 1 OF 3

3 11 D

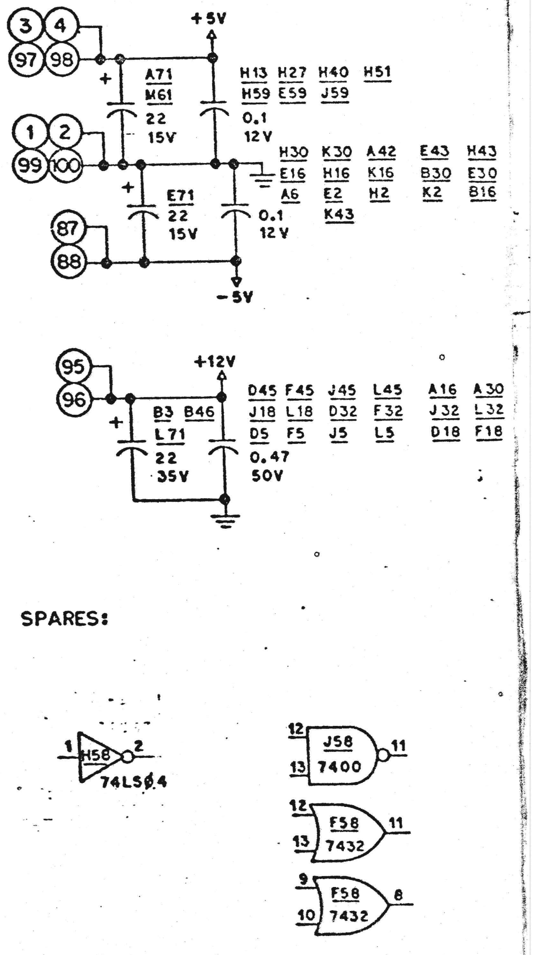
PRODUCT NO. 23412-XX

6


PRODUCT NO. 23402-XX
A59 74367
B58 74367
L58 74367
K58 74367
+ MEM ADDR Ø
+ MEM ADDR 1
+ MEM ADDR 2
+ MEM ADDR 3
+ MEM ADDR 4
+ MEM ADDR 5
+ MEM ADDR 6
+ MEM ADDR 7
+ MEM ADDR 8
+ MEM ADDR 9
+ MEM ADDR 10
+ MEM ADDR 11
+ MEM ADDR 12
+ MEM ADDR 13
+ MEM ADDR 14
+ MEM ADDR 15
– RFSH
– BOARD EN
+ MEM BUS EN
+ MEM DATA Ø
+ MEM DATA 1
+ MEM DATA 2
+ MEM DATA 3
+ MEM DATA 4
+ MEM DATA 5
+ MEM DATA 6
+ MEM DATA 7
+ MEM DATA 8
+ R/W̄
+ DATA Ø
+ DATA 1
+ DATA 2
+ DATA 3
+ DATA 4
+ DATA 5
+ DATA 6
+ DATA 7
+ DATA 8
+ CHIP EN
+ BUF MEM ADDR Ø
+ BUF MEM ADDR 1
+ BUF MEM ADDR 2
+ BUF MEM ADDR 3
+ BUF MEM ADDR 4
+ BUF MEM ADDR 5
+ BUF MEM ADDR 6
+ BUF MEM ADDR 7
+ BUF MEM ADDR 8
+ BUF MEM ADDR 9
+ BUF MEM ADDR 10
+ BUF MEM ADDR 11
CHIP SELECT
DCDR E58 9321
BOARD SELECT
– CS Ø
– CS 1
– CS 2
– CS 3
– SELECT Ø-16K
– SELECT 16-32K
– SELECT 32-48K
– SELECT 48-64K
– DATA Ø
– DATA 1
– DATA 2
– DATA 3
– DATA 4
– DATA 5
– DATA 6
– DATA 7
– DATA 8
74LSØ4
J58 7400
F58 7432
M58 75322
M49 9.1
K59 15
+ CHIP EN 1
+ CHIP EN 2
M66 A5T4260
M65 A5T4260
+ BUF R/W
+12V
SH2 ⅊ 3-K16
SH2 ⅊ 3-J16
SH2 ⅊ 3-H16
SH2-G16
SH2-C16
SH3-G16
SH3-C16
SH2 ⅊ 3-G16
SH2 ⅊ 3-F16
SH2-H16
SH3-H16
SH2 ⅊ 3-G3
SH2 ⅊ 3-F3

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ±5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN I.C., GND TO PIN 7; +5V TO PIN 16 OF 16-PIN I.C., GND TO PIN 8.
5. THESE SIGNALS CONNECT TO THE SAME PIN NUMBER SPECIFIED ON ALL RAM I.C.'S SHOWN ON THIS SHEET.
6. A DASH NUMBER DENOTES THE MEMORY CAPACITY IN 4K BYTE INCREMENTS OF 8 OR 9 BITS.
7. CHANGE TO 18 OHMS ON 23402-03 AND 23402-04.


+5V
A71 M61 22 15V
0.1 12V
H13 H27 H40 H51
H59 E59 J59
H30 K30 A42 E43 H43
E16 H16 K16 B30 E30
A6 E2 H2 K2 B16
K43
E71 22 15V
0.1 12V
-5V
+12V
B3 B46
L71
22 35V
0.47 50V
D45 F45 J45 L45 A16 A30
J18 L18 D32 F32 J32 L32
D5 F5 J5 L5 D18 F18
SPARES:
H58 74LSØ4
J58 7400
F58 7432

SCHEMATIC DIAGRAM

Diablo Systems Incorpora
Hayward, California 94545

TITLE PW ASSY, MEM Ø4

MODEL 23400

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SCHEMATIC INCLUDES SHEETS 1 THRU 3

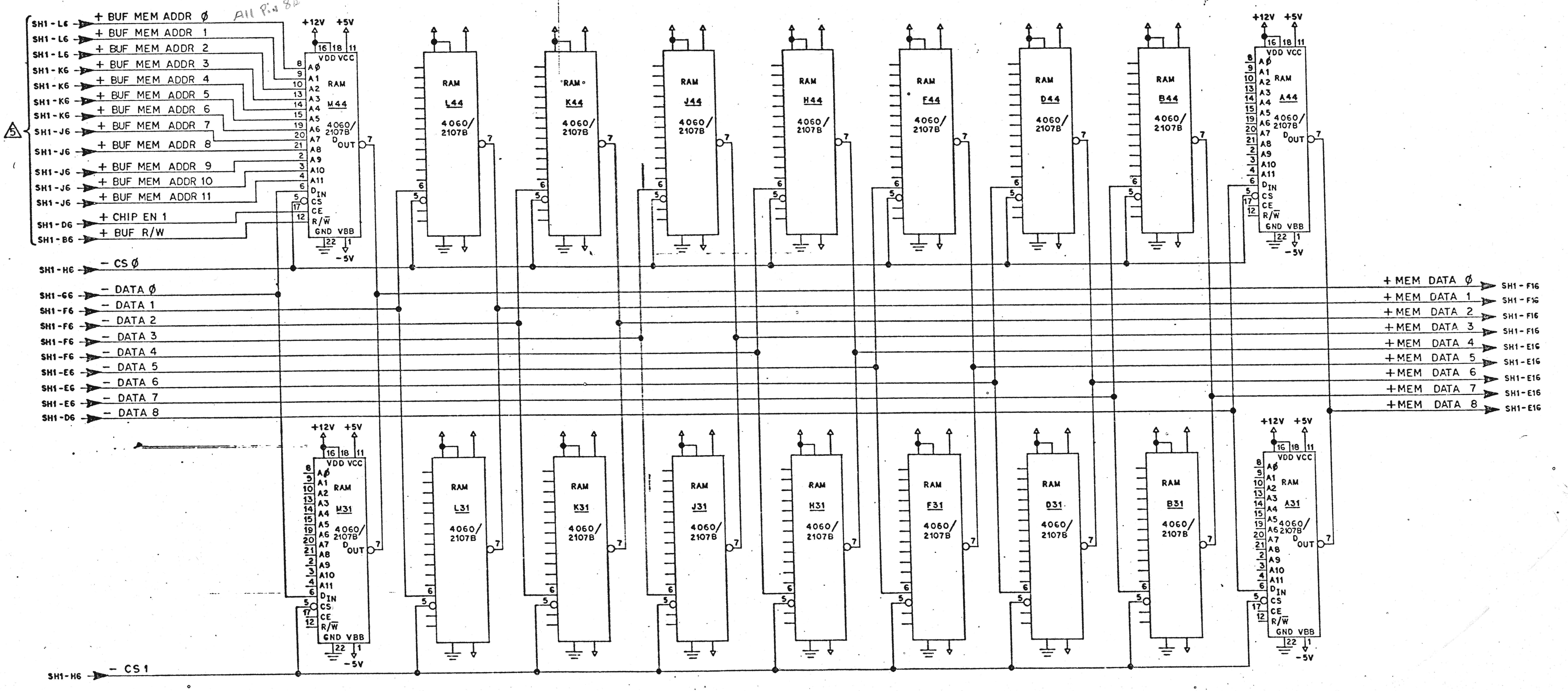
SHEET 1 TOTAL SHEETS 14 D

PRODUCT NO. 23402-XX

PRODUCT NO. 23402-XX

6-5-75

23402-XX



SH1-L6 + BUF MEM ADDR Ø
SH1-L6 + BUF MEM ADDR 1
SH1-L6 + BUF MEM ADDR 2
SH1-K6 + BUF MEM ADDR 3
SH1-K6 + BUF MEM ADDR 4
SH1-K6 + BUF MEM ADDR 5
SH1-K6 + BUF MEM ADDR 6
SH1-J6 + BUF MEM ADDR 7
SH1-J6 + BUF MEM ADDR 8
SH1-J6 + BUF MEM ADDR 9
SH1-J6 + BUF MEM ADDR 10
SH1-J6 + BUF MEM ADDR 11
SH1-D6 + CHIP EN 1
SH1-B6 + BUF R/W
All Pin 8's
5
SH1-H6 - CS Ø
SH1-G6 - DATA Ø
SH1-F6 - DATA 1
SH1-F6 - DATA 2
SH1-F6 - DATA 3
SH1-F6 - DATA 4
SH1-E6 - DATA 5
SH1-E6 - DATA 6
SH1-E6 - DATA 7
SH1-D6 - DATA 8
SH1-H6 - CS 1
+MEM DATA Ø SH1-F16
+MEM DATA 1 SH1-F16
+MEM DATA 2 SH1-F16
+MEM DATA 3 SH1-F16
+MEM DATA 4 SH1-E16
+MEM DATA 5 SH1-E16
+MEM DATA 6 SH1-E16
+MEM DATA 7 SH1-E16
+MEM DATA 8 SH1-E16
+12V +5V
VDD VCC
AØ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
DIN CS CE R/W
GND VBB
DOUT
-5V
RAM M44 4060/2107B
RAM L44 4060/2107B
RAM K44 4060/2107B
RAM J44 4060/2107B
RAM H44 4060/2107B
RAM F44 4060/2107B
RAM D44 4060/2107B
RAM B44 4060/2107B
RAM A44 4060/2107B
RAM M31 4060/2107B
RAM L31 4060/2107B
RAM K31 4060/2107B
RAM J31 4060/2107B
RAM H31 4060/2107B
RAM F31 4060/2107B
RAM D31 4060/2107B
RAM B31 4060/2107B
RAM A31 4060/2107B

SCHEMATIC DIAGRAM

Diablo Systems Incorpora
Hayward, California 94545

TITLE PW ASSY, MEM Ø4

MODEL 23400

SCHEMATIC INCLUDES SHEETS. 1 THRU 3

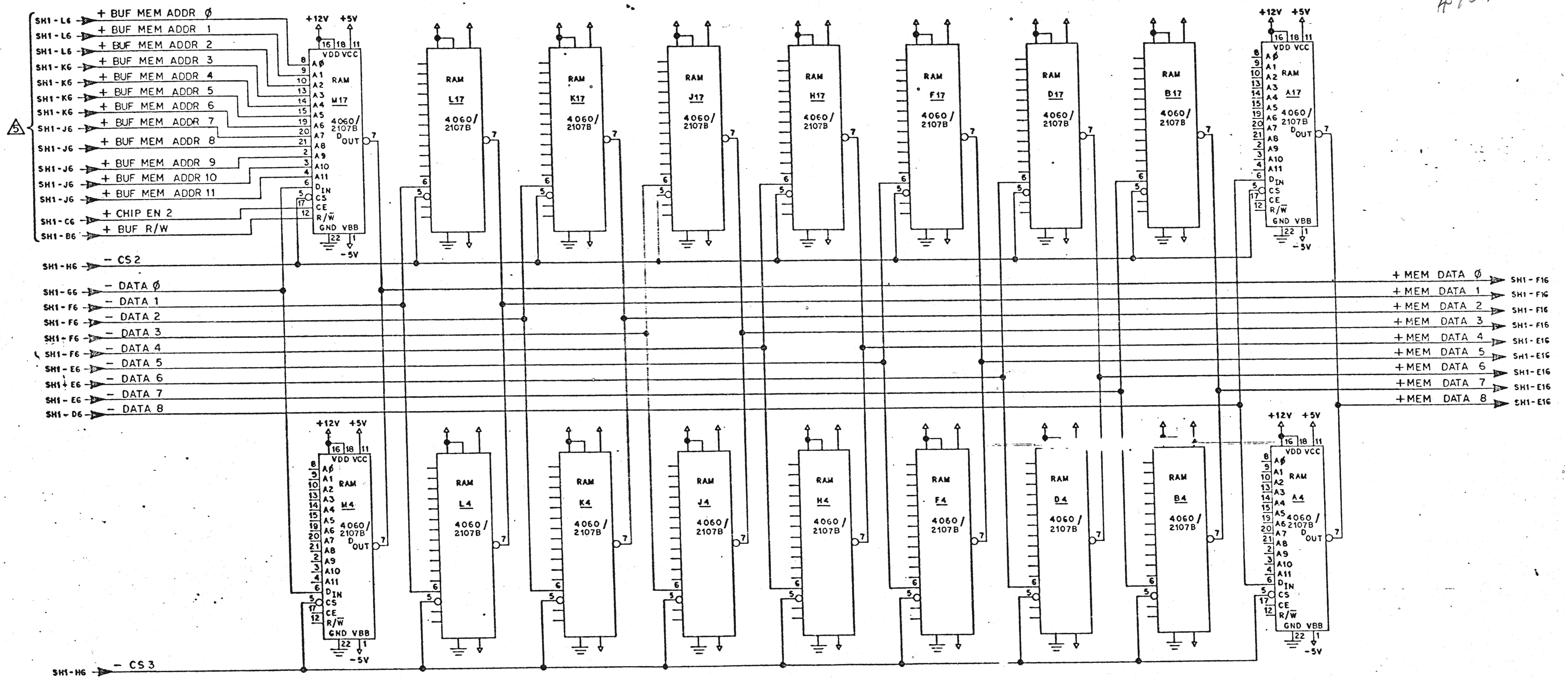
SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.
2	14	D	23402-XX

DATE	ENG DATE	CHECKED DATE	DRAWN DATE
5/28/76	5/28/76	5/27/7	5-29-75

DEVELOPMENT REV D

23402-XX

23402-XX


SH1-L6 + BUF MEM ADDR 0
SH1-L6 + BUF MEM ADDR 1
SH1-L6 + BUF MEM ADDR 2
SH1-K6 + BUF MEM ADDR 3
SH1-K6 + BUF MEM ADDR 4
SH1-K6 + BUF MEM ADDR 5
SH1-K6 + BUF MEM ADDR 6
SH1-J6 + BUF MEM ADDR 7
SH1-J6 + BUF MEM ADDR 8
SH1-J6 + BUF MEM ADDR 9
SH1-J6 + BUF MEM ADDR 10
SH1-J6 + BUF MEM ADDR 11
SH1-C6 + CHIP EN 2
SH1-B6 + BUF R/W
5
SH1-H6 − CS2
SH1-G6 − DATA 0
SH1-F6 − DATA 1
SH1-F6 − DATA 2
SH1-F6 − DATA 3
SH1-F6 − DATA 4
SH1-E6 − DATA 5
SH1-E6 − DATA 6
SH1-E6 − DATA 7
SH1-D6 − DATA 8
SH1-H6 − CS3
+MEM DATA 0 SH1-F16
+MEM DATA 1 SH1-F16
+MEM DATA 2 SH1-F16
+MEM DATA 3 SH1-F16
+MEM DATA 4 SH1-E16
+MEM DATA 5 SH1-E16
+MEM DATA 6 SH1-E16
+MEM DATA 7 SH1-E16
+MEM DATA 8 SH1-E16
+12V +5V
16 18 11
VDD VCC
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
DIN CS CE R/W
GND VBB
22 1
−5V
DOUT 7
RAM M17 4060/2107B
RAM L17 4060/2107B
RAM K17 4060/2107B
RAM J17 4060/2107B
RAM H17 4060/2107B
RAM F17 4060/2107B
RAM D17 4060/2107B
RAM B17 4060/2107B
RAM A17 4060/2107B
RAM M4 4060/2107B
RAM L4 4060/2107B
RAM K4 4060/2107B
RAM J4 4060/2107B
RAM H4 4060/2107B
RAM F4 4060/2107B
RAM D4 4060/2107B
RAM B4 4060/2107B
RAM A4 4060/2107B

470ma.

SCHEMATIC DIAGRAM

Diablo Systems Incorpora
Hayward California 94545

TITLE
PW ASSY, MEM 04

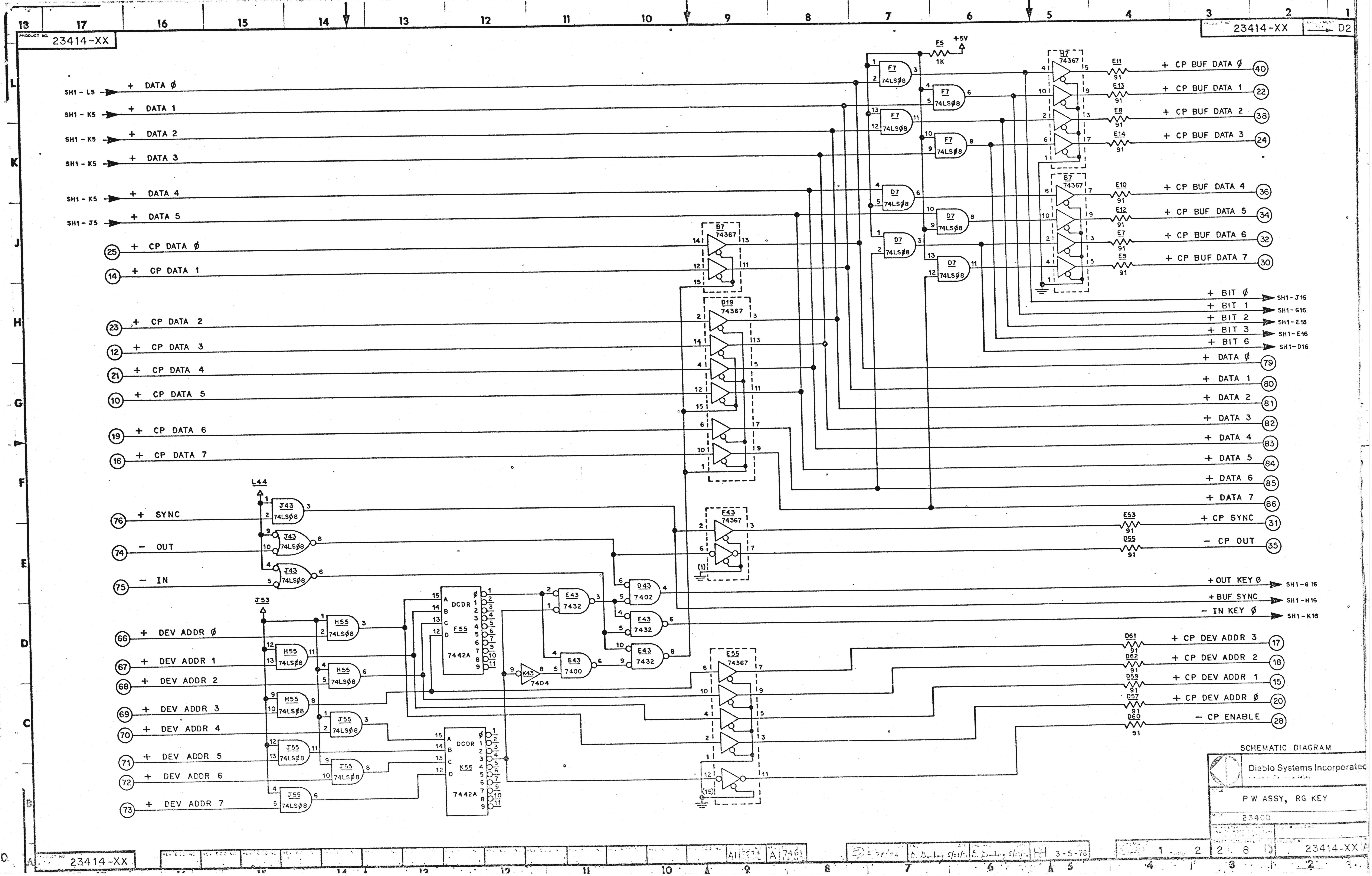
MODEL 23400

SCHEMATIC INCLUDES SHEETS 1 THRU 3
SHEET 3
TOTAL SHEETS 14
PRODUCT NO. 23402-XX

5-29-75

23402-XX

9


23414-XX
SH1 - L5 + DATA Ø
SH1 - K5 + DATA 1
SH1 - K5 + DATA 2
SH1 - K5 + DATA 3
SH1 - K5 + DATA 4
SH1 - J5 + DATA 5
25 + CP DATA Ø
14 + CP DATA 1
23 + CP DATA 2
12 + CP DATA 3
21 + CP DATA 4
10 + CP DATA 5
19 + CP DATA 6
16 + CP DATA 7
76 + SYNC
74 − OUT
75 − IN
66 + DEV ADDR Ø
67 + DEV ADDR 1
68 + DEV ADDR 2
69 + DEV ADDR 3
70 + DEV ADDR 4
71 + DEV ADDR 5
72 + DEV ADDR 6
73 + DEV ADDR 7
L44
J53
F7 74LSØ8
D7 74LSØ8
H7 74367
B7 74367
D19 74367
F43 74367
E55 74367
J43 74LSØ8
H55 74LSØ8
J55 74LSØ8
DCDR F55 7442A
DCDR K55 7442A
E43 7432
D43 7402
B43 7400
K43 7404
F5 1K +5V
E11 91
E13 91
E8 91
E14 91
E10 91
E12 91
E7 91
E9 91
E53 91
D55 91
D61 91
D62 91
D59 91
D57 91
D60 91
+ CP BUF DATA Ø 40
+ CP BUF DATA 1 22
+ CP BUF DATA 2 38
+ CP BUF DATA 3 24
+ CP BUF DATA 4 36
+ CP BUF DATA 5 34
+ CP BUF DATA 6 32
+ CP BUF DATA 7 30
+ BIT Ø SH1 - J16
+ BIT 1 SH1 - G16
+ BIT 2 SH1 - E16
+ BIT 3 SH1 - E16
+ BIT 6 SH1 - D16
+ DATA Ø 79
+ DATA 1 80
+ DATA 2 81
+ DATA 3 82
+ DATA 4 83
+ DATA 5 84
+ DATA 6 85
+ DATA 7 86
+ CP SYNC 31
− CP OUT 35
+ OUT KEY Ø SH1 - G 16
+ BUF SYNC SH1 - H16
− IN KEY Ø SH1 - K16
+ CP DEV ADDR 3 17
+ CP DEV ADDR 2 18
+ CP DEV ADDR 1 15
+ CP DEV ADDR Ø 20
− CP ENABLE 28
13 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
L K J H G F E D C
D2

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

P W ASSY, RG KEY

23400

23414-XX

A 7612 A 7461

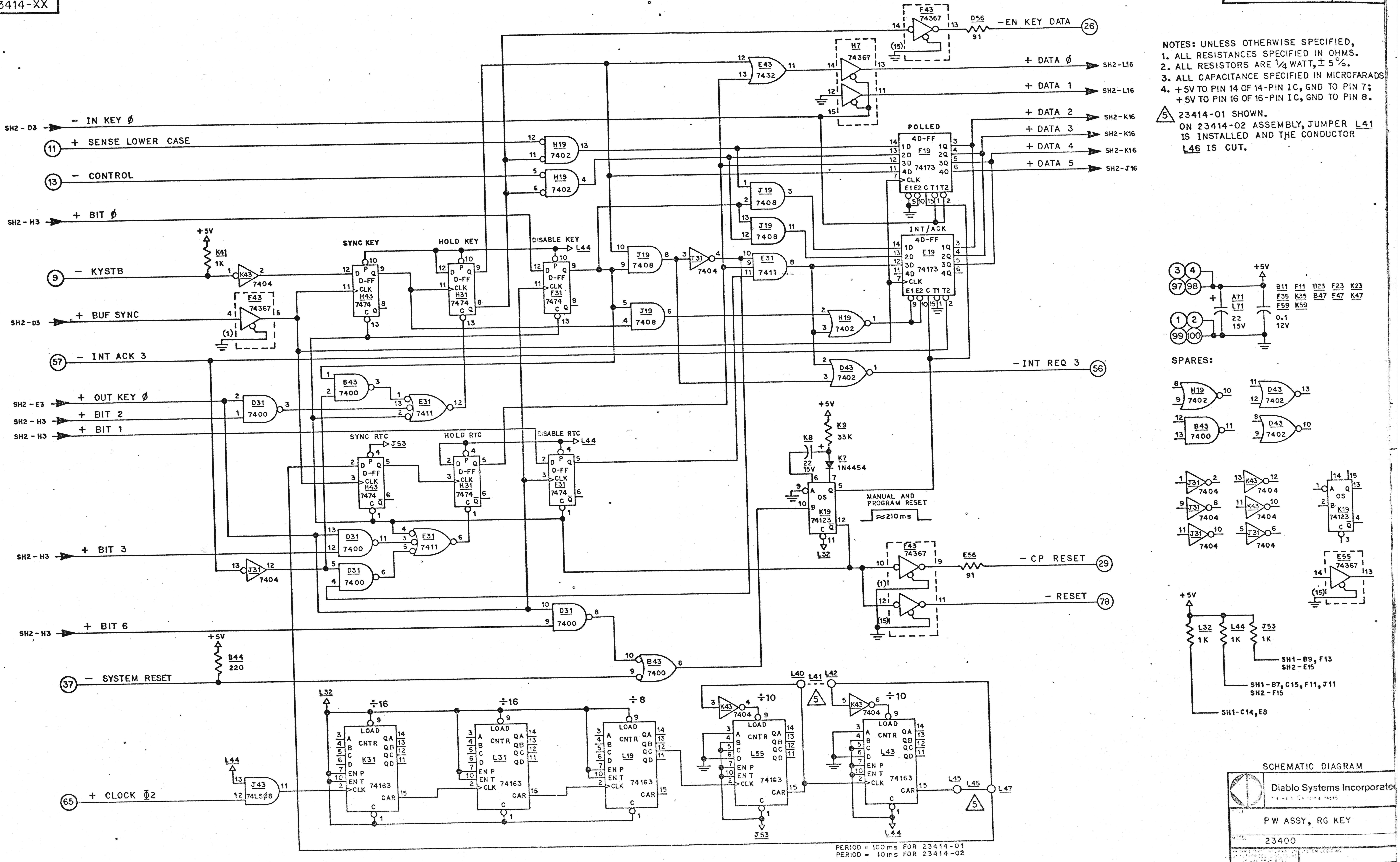
3-5-76

1 OF 2

2 8 D

23414-XX

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
⑤ 23414-01 SHOWN. ON 23414-02 ASSEMBLY, JUMPER L41 IS INSTALLED AND THE CONDUCTOR L46 IS CUT.



- EN KEY DATA
+ DATA 0
+ DATA 1
+ DATA 2
+ DATA 3
+ DATA 4
+ DATA 5
- IN KEY 0
+ SENSE LOWER CASE
- CONTROL
+ BIT 0
- KYSTB
+ BUF SYNC
- INT ACK 3
+ OUT KEY 0
+ BIT 2
+ BIT 1
+ BIT 3
+ BIT 6
- SYSTEM RESET
+ CLOCK Φ2
- INT REQ 3
- CP RESET
- RESET
SYNC KEY
HOLD KEY
DISABLE KEY
SYNC RTC
HOLD RTC
DISABLE RTC
POLLED 4D-FF
INT/ACK 4D-FF
MANUAL AND PROGRAM RESET
≈210ms
SPARES:
÷16
÷16
÷8
÷10
÷10

PERIOD = 100ms FOR 23414-01
PERIOD = 10ms FOR 23414-02

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG KEY

MODEL 23400

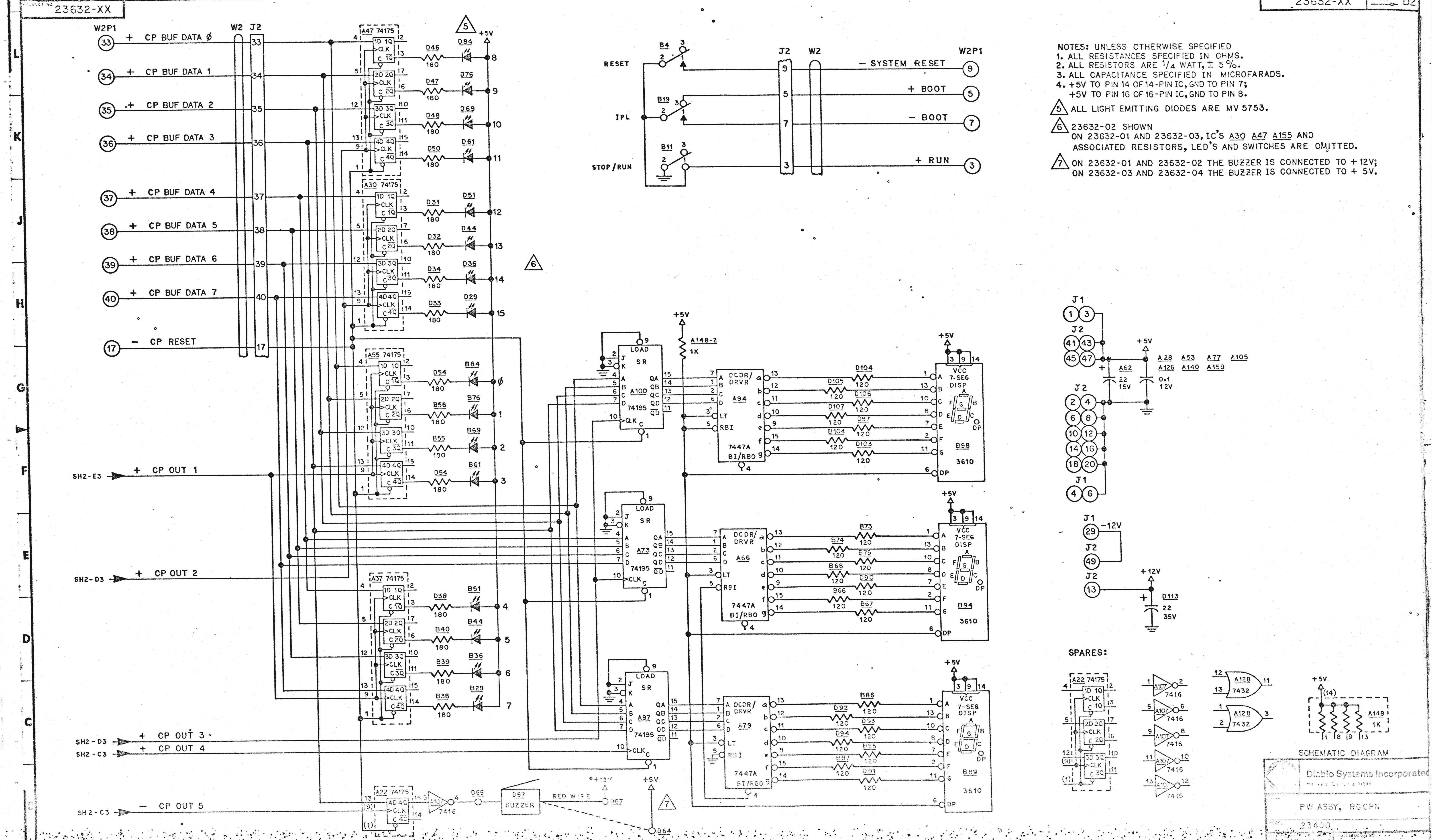
SCHEMATIC INCLUDES SHEETS 1 THRU 2

SHEET 1 TOTAL SHEETS 8 SIZE D

PRODUCT NO. 23414-XX

3-1-76

23414-XX


23632-XX
W2P1
W2 J2
+ CP BUF DATA 0
+ CP BUF DATA 1
+ CP BUF DATA 2
+ CP BUF DATA 3
+ CP BUF DATA 4
+ CP BUF DATA 5
+ CP BUF DATA 6
+ CP BUF DATA 7
- CP RESET
A47 74175
A30 74175
A55 74175
A37 74175
A22 74175
+5V
SH2-E3 + CP OUT 1
SH2-D3 + CP OUT 2
SH2-D3 + CP OUT 3
SH2-C3 + CP OUT 4
SH2-C3 - CP OUT 5
RESET
IPL
STOP/RUN
B4
B19
B11
- SYSTEM RESET
+ BOOT
- BOOT
+ RUN
LOAD SR
A100 74195
A73 74195
A87 74195
DCDR/DRVR
A94
A66
A79
7447A
BI/RBO
LT
RBI
A148-2 1K
VCC 7-SEG DISP
B98 3610
B94 3610
B89 3610
A107 7416
D57 BUZZER
RED WIRE
D64
D67
J1
J2
A62 22 15V
0.1 12V
A28 A53 A77 A105
A126 A140 A159
-12V
+12V
D113 22 35V
SPARES:
A128 7432
A148 1K

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
+5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. ALL LIGHT EMITTING DIODES ARE MV 5753.
6. 23632-02 SHOWN
ON 23632-01 AND 23632-03, IC'S A30 A47 A155 AND ASSOCIATED RESISTORS, LED'S AND SWITCHES ARE OMITTED.
7. ON 23632-01 AND 23632-03 THE BUZZER IS CONNECTED TO + 12V;
ON 23632-03 AND 23632-04 THE BUZZER IS CONNECTED TO + 5V.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RGCPN

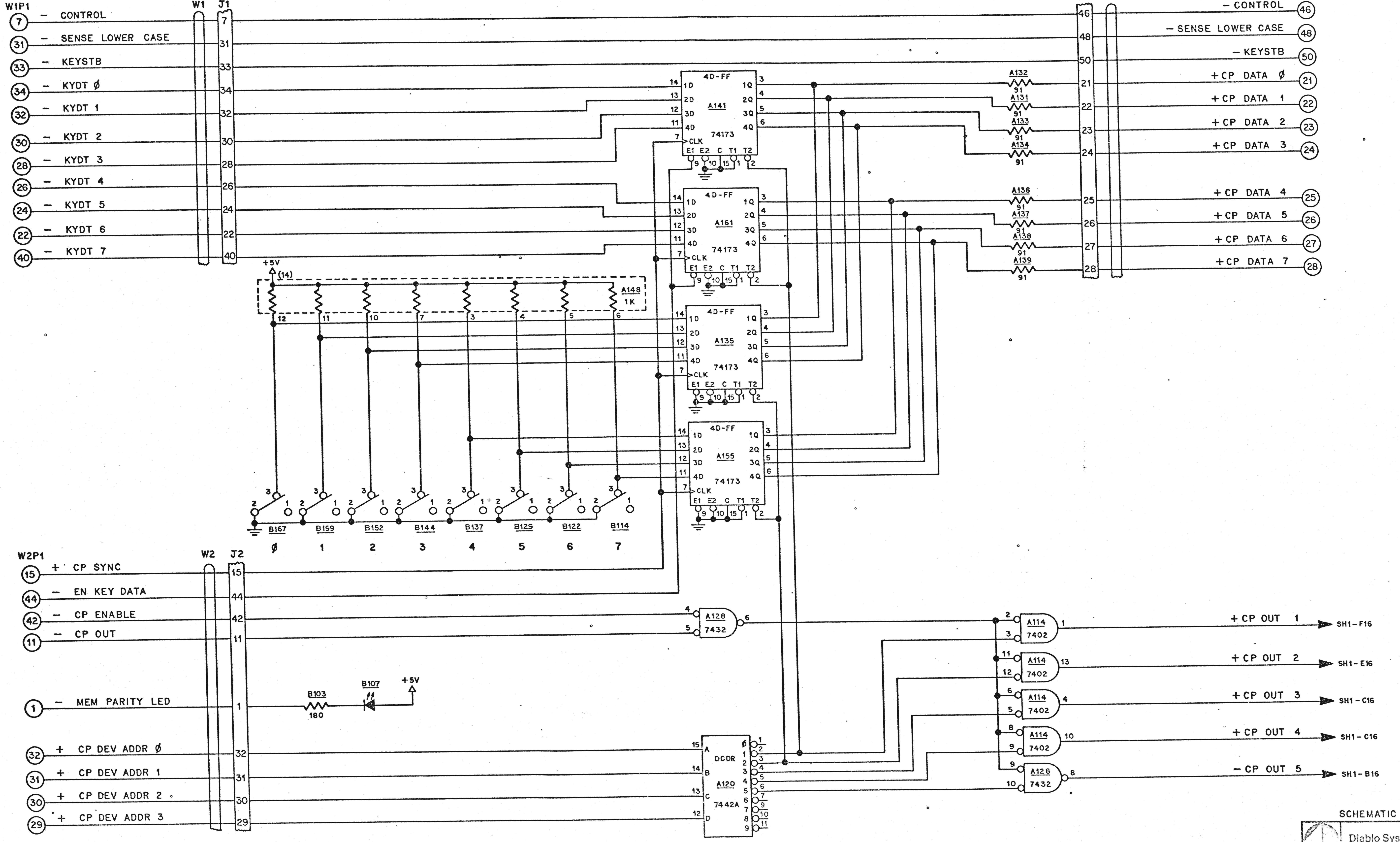
23400

3-15-76

1 2 1 11

23632-XX

12


W1P1
W1
J1
7 – CONTROL
31 – SENSE LOWER CASE
33 – KEYSTB
34 – KYDT Ø
32 – KYDT 1
30 – KYDT 2
28 – KYDT 3
26 – KYDT 4
24 – KYDT 5
22 – KYDT 6
40 – KYDT 7
J2
W2
W2P1
– CONTROL 46
– SENSE LOWER CASE 48
– KEYSTB 50
+ CP DATA Ø 21
+ CP DATA 1 22
+ CP DATA 2 23
+ CP DATA 3 24
+ CP DATA 4 25
+ CP DATA 5 26
+ CP DATA 6 27
+ CP DATA 7 28
A132 91
A131 91
A133 91
A134 91
A136 91
A137 91
A138 91
A139 91
4D-FF
A141
74173
A161
74173
A135
74173
A155
74173
1D
2D
3D
4D
CLK
1Q
2Q
3Q
4Q
E1 E2 C T1 T2
+5V
(14)
A148
1K
B167
B159
B152
B144
B137
B129
B122
B114
Ø
1
2
3
4
5
6
7
W2P1
W2
J2
15 + CP SYNC
44 – EN KEY DATA
42 – CP ENABLE
11 – CP OUT
1 – MEM PARITY LED
B103
180
B107
+5V
32 + CP DEV ADDR Ø
31 + CP DEV ADDR 1
30 + CP DEV ADDR 2
29 + CP DEV ADDR 3
A128
7432
DCDR
A120
7442A
A114
7402
A114
7402
A114
7402
A114
7402
A128
7432
+ CP OUT 1 SH1-F16
+ CP OUT 2 SH1-E16
+ CP OUT 3 SH1-C16
+ CP OUT 4 SH1-C16
– CP OUT 5 SH1-B16

SCHEMATIC DIAGRAM

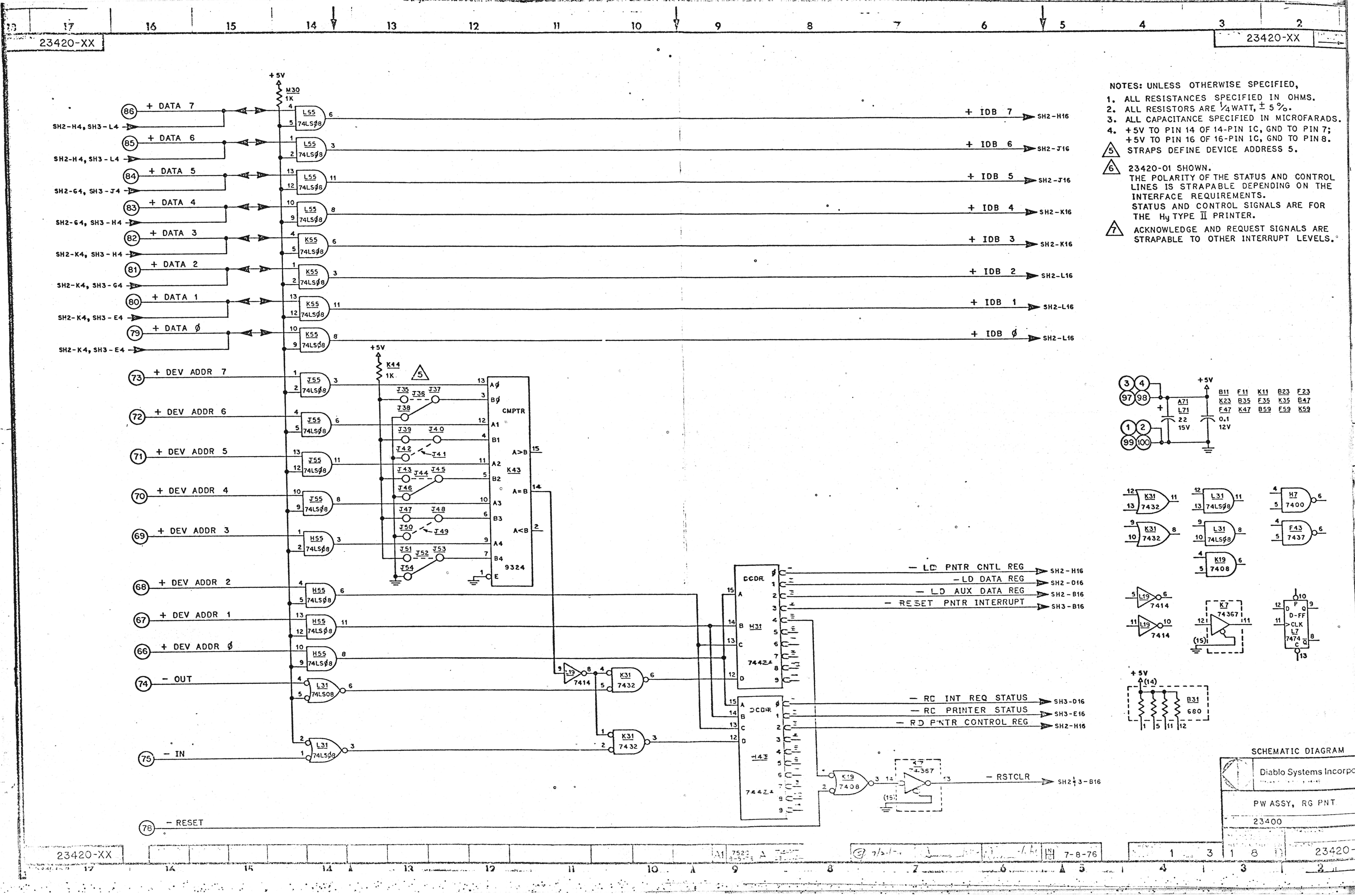
Diablo Systems Incorporate
Hayward California 94545

TITLE
PW ASSY RGCPN

MODEL
23400

SCHEMATIC SHEETS 1 THRU 2
SHEET 2
TOTAL SHEETS 11
PRODUCT NO 23632-XX

A 7519
3-17-76


23420-XX
+5V
M30
1K
+ DATA 7
+ DATA 6
+ DATA 5
+ DATA 4
+ DATA 3
+ DATA 2
+ DATA 1
+ DATA Ø
SH2-H4, SH3-L4
SH2-G4, SH3-J4
SH2-G4, SH3-H4
SH2-K4, SH3-H4
SH2-K4, SH3-G4
SH2-K4, SH3-E4
L55
K55
74LSØ8
+ IDB 7
+ IDB 6
+ IDB 5
+ IDB 4
+ IDB 3
+ IDB 2
+ IDB 1
+ IDB Ø
SH2-H16
SH2-J16
SH2-K16
SH2-L16
+ DEV ADDR 7
+ DEV ADDR 6
+ DEV ADDR 5
+ DEV ADDR 4
+ DEV ADDR 3
+ DEV ADDR 2
+ DEV ADDR 1
+ DEV ADDR Ø
J55
H55
K44
1K
J35 J36 J37 J38 J39 J40 J41 J42 J43 J44 J45 J46 J47 J48 J49 J50 J51 J52 J53 J54
CMPTR
K43
9324
A>B
A=B
A<B
- OUT
- IN
- RESET
L31
74LS08
L19
7414
K31
7432
DCDR
H31
H43
7442A
- LD PNTR CNTL REG
- LD DATA REG
- LD AUX DATA REG
- RESET PNTR INTERRUPT
SH2-D16
SH2-B16
SH3-B16
- RC INT REQ STATUS
- RC PRINTER STATUS
- RD PNTR CONTROL REG
SH3-D16
SH3-E16
K19
7408
K7
74367
- RSTCLR
SH2/3-B16
B11 F11 K11 B23 F23
K23 B35 F35 K35 B47
F47 K47 B59 F59 K59
A71
L71
22
15V
0.1
12V
H7
7400
F43
7437
L7
7474
D-FF
B31
680
7-8-76

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

⚠5 STRAPS DEFINE DEVICE ADDRESS 5.

⚠6 23420-01 SHOWN. THE POLARITY OF THE STATUS AND CONTROL LINES IS STRAPABLE DEPENDING ON THE INTERFACE REQUIREMENTS. STATUS AND CONTROL SIGNALS ARE FOR THE Hy TYPE II PRINTER.

⚠7 ACKNOWLEDGE AND REQUEST SIGNALS ARE STRAPABLE TO OTHER INTERRUPT LEVELS.

SCHEMATIC DIAGRAM

Diablo Systems Incorpo

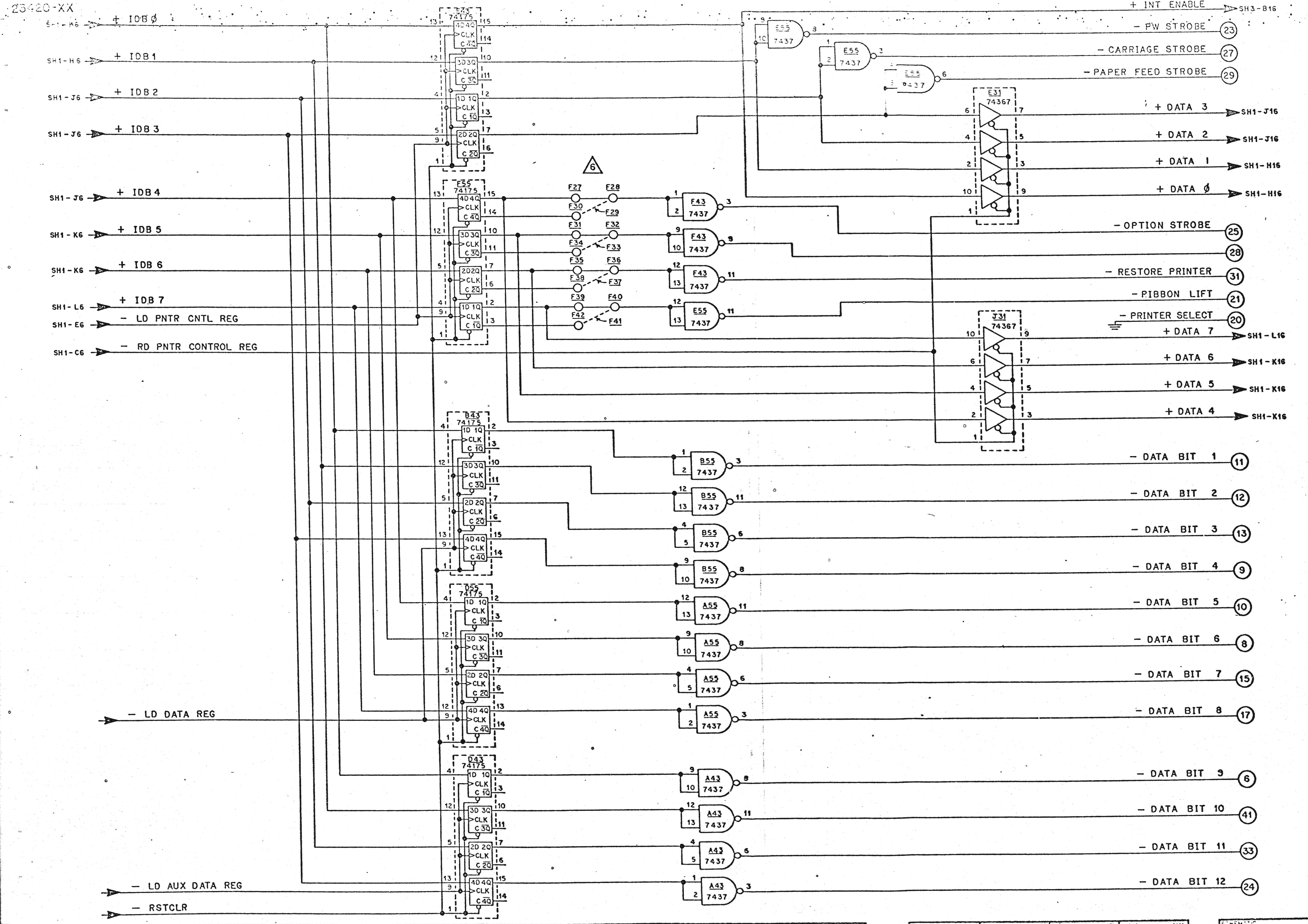
PW ASSY, RG PNT

23400

1 3

1 8

23420-


23420-XX
SH1-H6 + IDB 0
SH1-H6 + IDB 1
SH1-J6 + IDB 2
SH1-J6 + IDB 3
SH1-J6 + IDB 4
SH1-K6 + IDB 5
SH1-K6 + IDB 6
SH1-L6 + IDB 7
SH1-E6 - LD PNTR CNTL REG
SH1-C6 - RD PNTR CONTROL REG
- LD DATA REG
- LD AUX DATA REG
- RSTCLR
E43 74175
E55 74175
B43 74175
D55 74175
D43 74175
E55 7437
E31 74367
J31 74367
F43 7437
B55 7437
A55 7437
A43 7437
F27 F28 F29 F30 F31 F32 F33 F34 F35 F36 F37 F38 F39 F40 F41 F42
6
+ INT ENABLE SH3-B16
- PW STROBE 23
- CARRIAGE STROBE 27
- PAPER FEED STROBE 29
+ DATA 3 SH1-J16
+ DATA 2 SH1-J16
+ DATA 1 SH1-H16
+ DATA 0 SH1-H16
- OPTION STROBE 25
28
- RESTORE PRINTER 31
- RIBBON LIFT 21
- PRINTER SELECT 20
+ DATA 7 SH1-L16
+ DATA 6 SH1-K16
+ DATA 5 SH1-K16
+ DATA 4 SH1-K16
- DATA BIT 1 11
- DATA BIT 2 12
- DATA BIT 3 13
- DATA BIT 4 9
- DATA BIT 5 10
- DATA BIT 6 8
- DATA BIT 7 15
- DATA BIT 8 17
- DATA BIT 9 6
- DATA BIT 10 41
- DATA BIT 11 33
- DATA BIT 12 24

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

Hayward, California 94545

PW ASSY, RG PNT

23400

A1 7520 8-5-76 A 7497

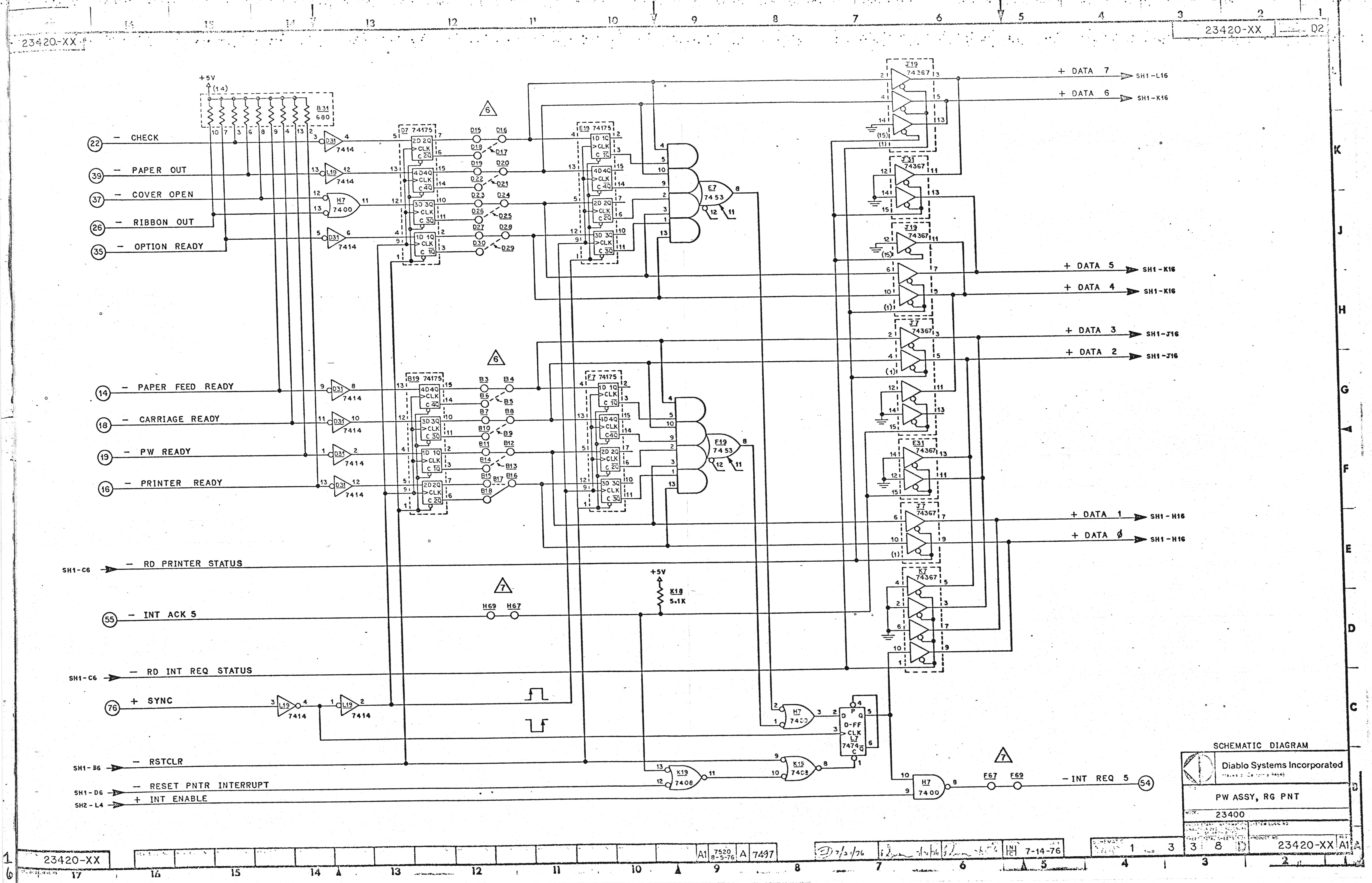
7/21/76

N/C 7-9-76

SCHEMATIC SHEETS 1 THRU 3

2 8 D

23420-XX A1 A



23420-XX
D2
+5V
(14)
B31
680
6
7
CHECK
PAPER OUT
COVER OPEN
RIBBON OUT
OPTION READY
22
39
37
26
35
D31
7414
L19
H7
7400
D7 74175
D15
D16
D18
D17
D19
D20
D22
D21
D23
D24
D26
D25
D27
D28
D30
D29
E19 74175
E7
7453
J19
74367
J31
74367
J7
74367
E31
74367
K7
74367
+ DATA 7
SH1-L16
+ DATA 6
SH1-K16
+ DATA 5
SH1-K16
+ DATA 4
SH1-K16
+ DATA 3
SH1-J16
+ DATA 2
SH1-J16
+ DATA 1
SH1-H16
+ DATA 0
SH1-H16
PAPER FEED READY
CARRIAGE READY
PW READY
PRINTER READY
14
18
19
16
B19 74175
B3
B4
B6
B5
B7
B8
B10
B9
B11
B12
B14
B13
B15
B17
B16
B18
F7 74175
F19
7453
RD PRINTER STATUS
SH1-C6
K18
5.1K
H69
H67
INT ACK 5
55
RD INT REQ STATUS
SH1-C6
+ SYNC
76
L19
7414
RSTCLR
SH1-B6
RESET PNTR INTERRUPT
SH1-D6
+ INT ENABLE
SH2-L4
K19
7408
D-FF
CLK
L7
7474
H7
7400
F67
F69
- INT REQ 5
54
A1
7520
8-5-76
A
7497
7/21/76
7-14-76

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG PNT

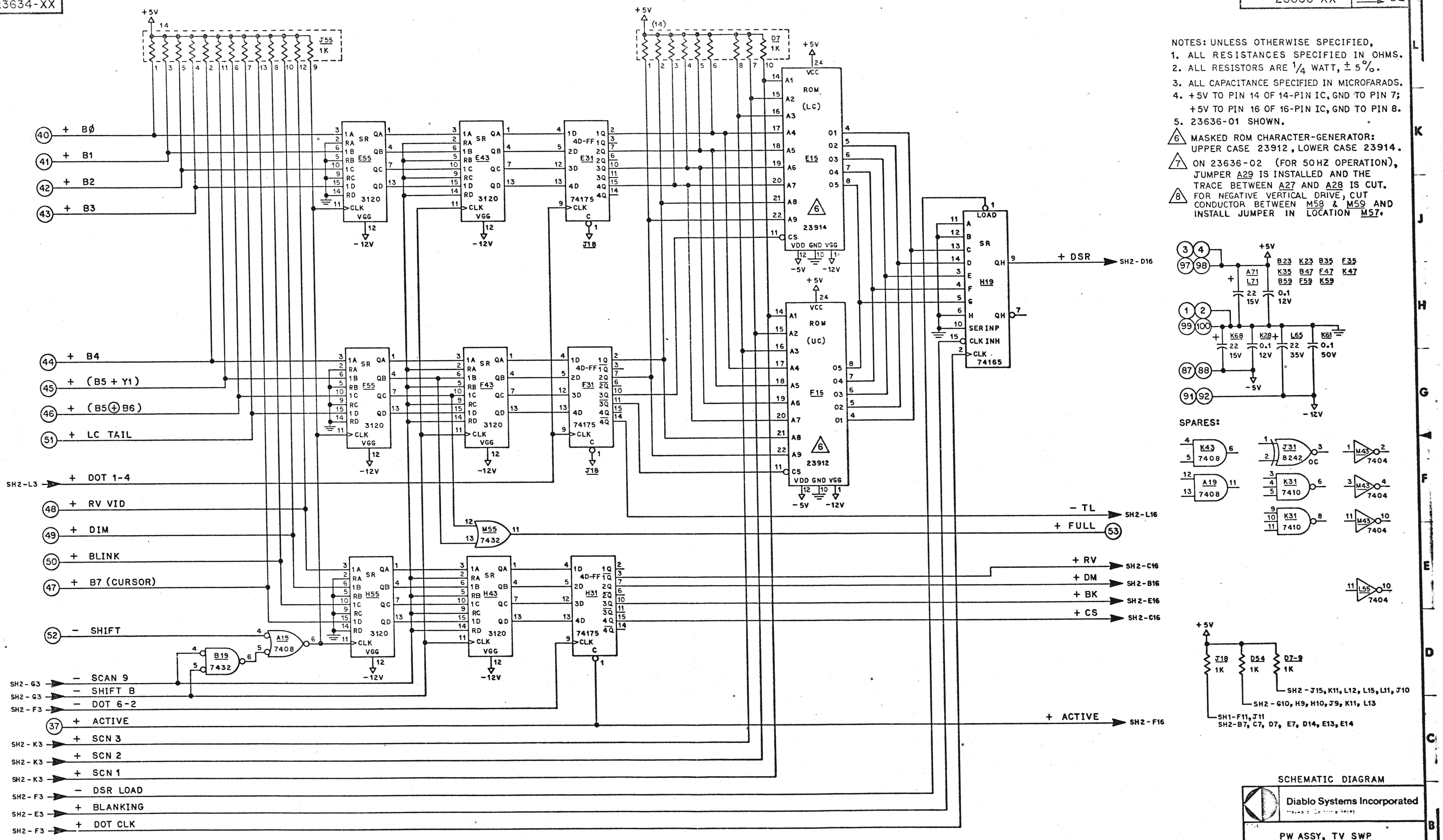
MODEL 23400

SCHEMATIC 1 THRU 3

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
3	8	D	23420-XX	A1

23634-XX

23636-XX D2



+5V
J55 1K
D7 1K
(40) + B0
(41) + B1
(42) + B2
(43) + B3
(44) + B4
(45) + (B5 + Y1)
(46) + (B5⊕B6)
(51) + LC TAIL
SH2-L3 + DOT 1-4
(48) + RV VID
(49) + DIM
(50) + BLINK
(47) + B7 (CURSOR)
(52) − SHIFT
SH2-G3 − SCAN 9
SH2-G3 − SHIFT B
SH2-F3 − DOT 6-2
(37) + ACTIVE
SH2-K3 + SCN 3
SH2-K3 + SCN 2
SH2-K3 + SCN 1
SH2-F3 − DSR LOAD
SH2-E3 + BLANKING
SH2-F3 + DOT CLK
E55 3120
E43 3120
E31 74175
F55 3120
F43 3120
F31 74175
H55 3120
H43 3120
H31 74175
−12V
J18
A19 7408
B19 7432
M55 7432
ROM (LC) E15 23914
ROM (UC) F15 23912
H19 74165
+ DSR SH2-D16
− TL SH2-L16
+ FULL (53)
+ RV SH2-C16
+ DM SH2-B16
+ BK SH2-E16
+ CS SH2-C16
+ ACTIVE SH2-F16
(3)(4) (97)(98)
(1)(2) (99)(100)
(87)(88)
(91)(92)
A71 L71 22 15V
B23 K23 B35 F35
K35 B47 F47 K47
B59 F59 K59
0.1 12V
K68 22 15V
K28 0.1 12V
L65 22 35V
K61 0.1 50V
−5V
−12V
SPARES:
K43 7408
A19 7408
J31 8242 OC
K31 7410
K31 7410
M43 7404
M43 7404
M43 7404
L55 7404
J18 1K
D54 1K
D7-9 1K
SH2-J15, K11, L12, L15, L11, J10
SH2-G10, H9, H10, J9, K11, L13
SH1-F11, J11
SH2-B7, C7, D7, E7, D14, E13, E14

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
+5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. 23636-01 SHOWN.
6. MASKED ROM CHARACTER-GENERATOR: UPPER CASE 23912, LOWER CASE 23914.
7. ON 23636-02 (FOR 50HZ OPERATION), JUMPER A29 IS INSTALLED AND THE TRACE BETWEEN A27 AND A28 IS CUT.
8. FOR NEGATIVE VERTICAL DRIVE, CUT CONDUCTOR BETWEEN M58 & M59 AND INSTALL JUMPER IN LOCATION M57.

SCHEMATIC DIAGRAM

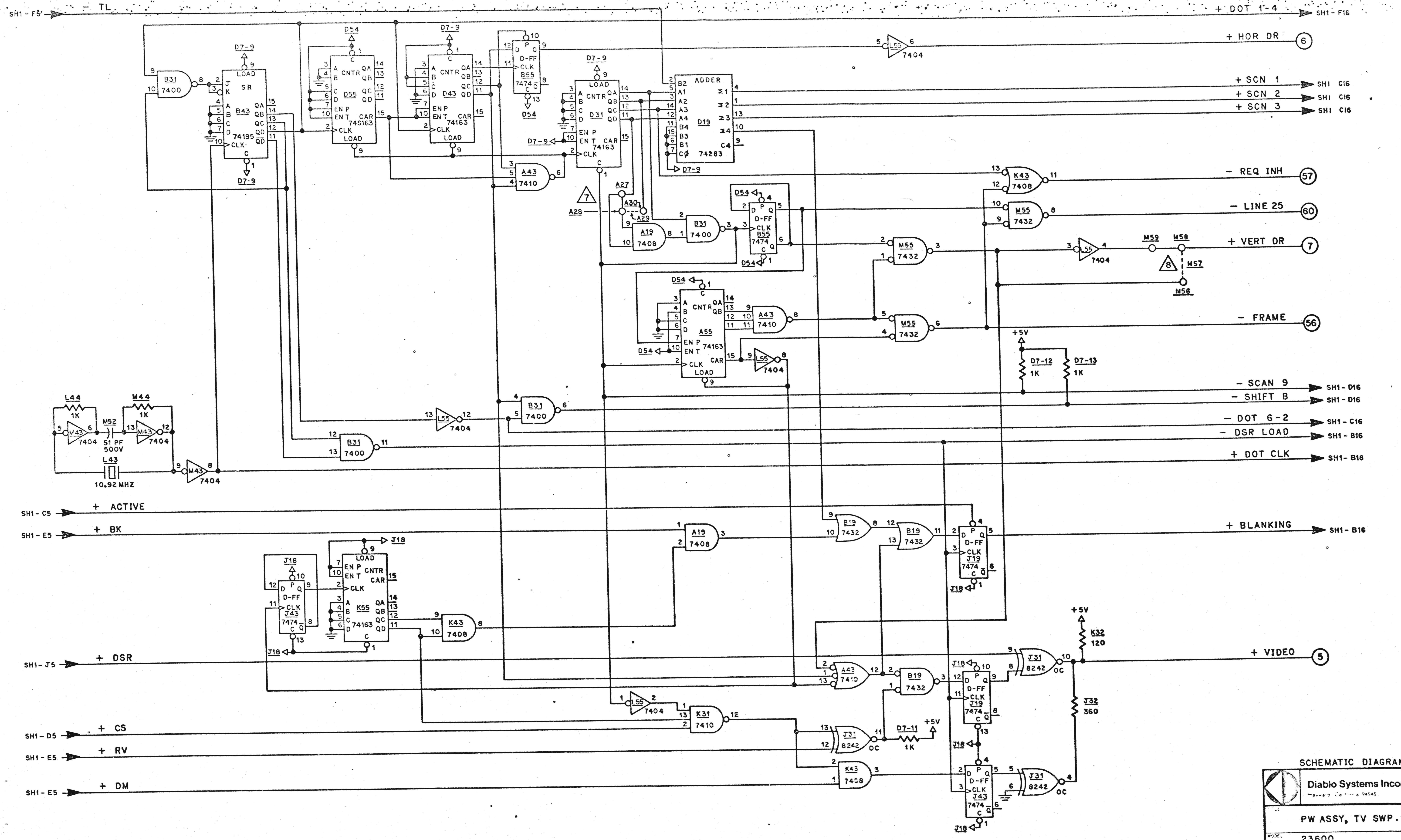
Diablo Systems Incorporated
Hayward, California 94545

TITLE PW ASSY, TV SWP
MODEL 23600
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED
SYSTEM LOGIC NO
SCHEMATIC INCLUDES SHEETS 1 THRU 2
SHEET 1 | TOTAL SHEETS 8 | SIZE D
PRODUCT NO 23634-XX | REV B

B 7578 10-27-76 | A 7518 8-6-76

Booth | Bowen 7-30-76 | 7/31/76 | N/C 6-23-76

PRODUCT NO 23634-XX



SH1-F5 – TL
+ DOT 1-4 SH1-F16
+ HOR DR ⑥
+ SCN 1 SH1 C16
+ SCN 2 SH1 C16
+ SCN 3 SH1 C16
– REQ INH (57)
– LINE 25 (60)
+ VERT DR ⑦
– FRAME (56)
– SCAN 9 SH1-D16
– SHIFT B SH1-D16
– DOT 6-2 SH1-C16
– DSR LOAD SH1-B16
+ DOT CLK SH1-B16
SH1-C5 + ACTIVE
SH1-E5 + BK
+ BLANKING SH1-B16
SH1-J5 + DSR
+ VIDEO ⑤
SH1-D5 + CS
SH1-E5 + RV
SH1-E5 + DM
B31 7400
B43 74195 SR
D55 74S163 CNTR
D43 74163 CNTR
B55 7474 D-FF
D31 74163 CNTR
D19 74283 ADDER
L55 7404
A43 7410
K43 7408
M55 7432
A19 7408
B31 7400
B55 7474
A55 74163
A27 A30 A29 A28
M59 M58 M57 M56
D7-12 1K
D7-13 1K
+5V
L44 1K
M44 1K
M43 7404
M52 51 PF 500V
L43 10.92 MHZ
B19 7432
J19 7474
J18
J43 7474 D-FF
K55 74163 CNTR
K31 7410
J31 8242
D7-11 1K
K32 120
J32 360
D54
D7-9

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

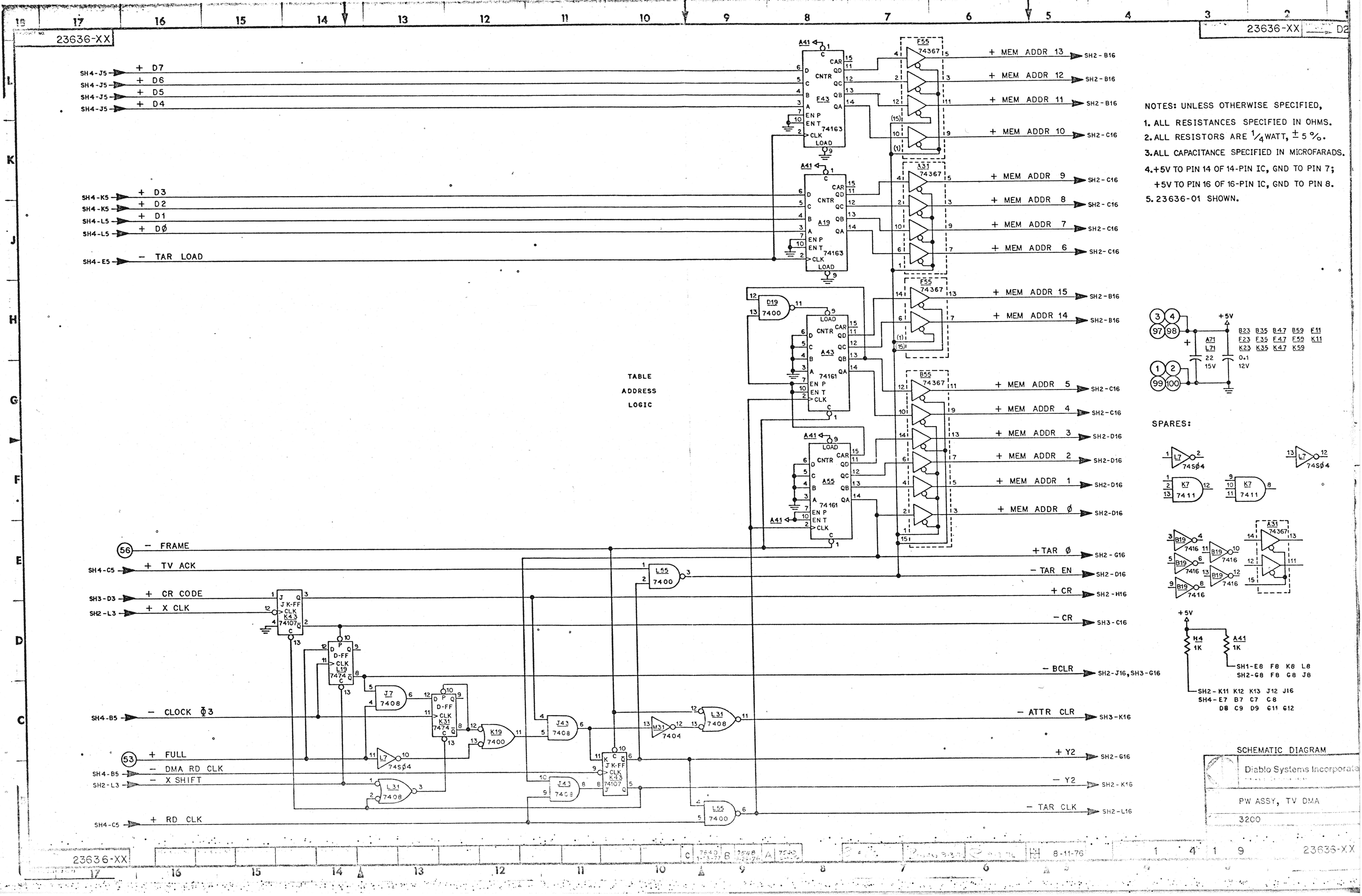
PW ASSY, TV SWP.

MODEL	23600
SHEET / TOTAL SHEETS / SIZE	2 / 8 / D
PRODUCT NO.	23634-XX
REV	B
SCHEMATIC SHEETS	1 THRU 2
DATE	6-30-76

B 7578 10-22-76

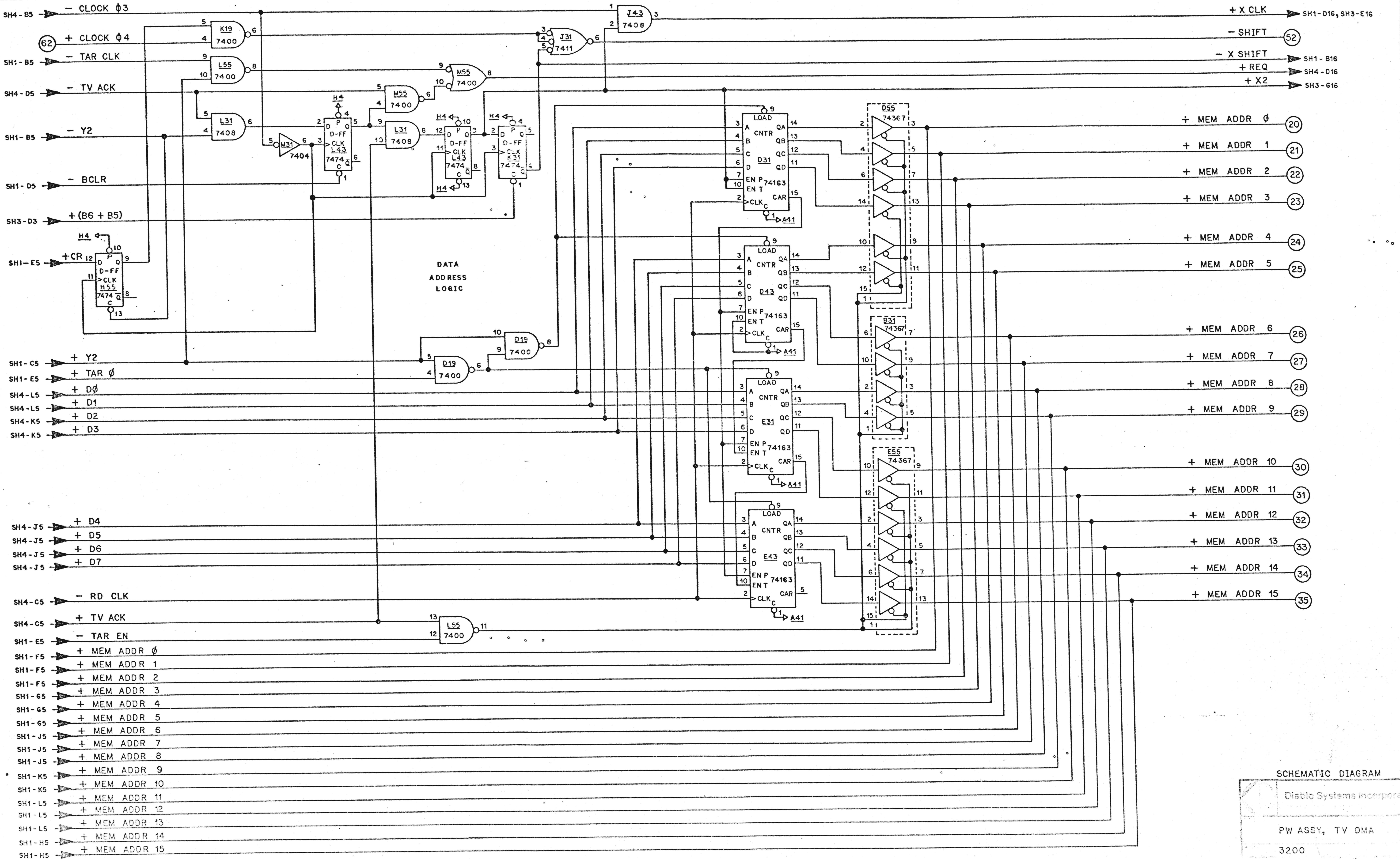
A 7513 8-4-76

Booth 3JUL76 Brown 7-30-76 L. ... 7/13/76


23636-XX
SH4-J5 + D7
SH4-J5 + D6
SH4-J5 + D5
SH4-J5 + D4
SH4-K5 + D3
SH4-K5 + D2
SH4-L5 + D1
SH4-L5 + D0
SH4-E5 − TAR LOAD
F43 74163
A19 74163
A43 74161
A55 74161
D19 7400
A41
F55 74367
A31 74367
B55 74367
+ MEM ADDR 13 SH2-B16
+ MEM ADDR 12 SH2-B16
+ MEM ADDR 11 SH2-B16
+ MEM ADDR 10 SH2-C16
+ MEM ADDR 9 SH2-C16
+ MEM ADDR 8 SH2-C16
+ MEM ADDR 7 SH2-C16
+ MEM ADDR 6 SH2-C16
+ MEM ADDR 15 SH2-B16
+ MEM ADDR 14 SH2-B16
+ MEM ADDR 5 SH2-C16
+ MEM ADDR 4 SH2-C16
+ MEM ADDR 3 SH2-D16
+ MEM ADDR 2 SH2-D16
+ MEM ADDR 1 SH2-D16
+ MEM ADDR 0 SH2-D16
TABLE ADDRESS LOGIC
56 − FRAME
SH4-C5 + TV ACK
SH3-D3 + CR CODE
SH2-L3 + X CLK
SH4-B5 − CLOCK Φ3
53 + FULL
SH4-B5 − DMA RD CLK
SH2-L3 − X SHIFT
SH4-C5 + RD CLK
K43 74107
L19 7474
J7 7408
K31 7474
K19 7400
L7 74S04
L31 7408
J43 7408
M31 7404
L55 7400
K13 74107
+TAR 0 SH2-G16
− TAR EN SH2-D16
+ CR SH2-H16
− CR SH3-C16
− BCLR SH2-J16, SH3-G16
− ATTR CLR SH3-K16
+ Y2 SH2-G16
− Y2 SH2-K16
− TAR CLK SH2-L16
+5V
A71 L71 22 15V
0.1 12V
B23 B35 B47 B59 F11
F23 F35 F47 F59 K11
K23 K35 K47 K59
SPARES:
L7 74S04
K7 7411
B19 7416
A31 74367
H4 1K
A41 1K
SH1-E8 F8 K8 L8
SH2-G8 F8 G8 J8
SH2-K11 K12 K13 J12 J16
SH4-E7 B7 C7 C8
D8 C9 D9 G11 G12
8-11-76

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5 %.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. 23636-01 SHOWN.

SCHEMATIC DIAGRAM
Diablo Systems Incorporated
PW ASSY, TV DMA
3200
23636-XX


SH4-B5 — CLOCK Ø3
62 + CLOCK Ø4
SH1-B5 — TAR CLK
SH4-D5 — TV ACK
SH1-B5 — Y2
SH1-D5 — BCLR
SH3-D3 + (B6 + B5)
SH1-E5 +CR
K19 7400
L55 7400
L31 7408
M31 7404
L43 7474 D-FF
H4
M55 7400
L31 7408
K31 7474 D-FF
J31 7411
J43 7408
H55 7474 D-FF
DATA ADDRESS LOGIC
D19 7400
SH1-C5 + Y2
SH1-E5 + TAR Ø
SH4-L5 + DØ
SH4-L5 + D1
SH4-K5 + D2
SH4-K5 + D3
SH4-J5 + D4
SH4-J5 + D5
SH4-J5 + D6
SH4-J5 + D7
SH4-C5 — RD CLK
SH4-C5 + TV ACK
SH1-E5 — TAR EN
L55 7400
D31 74163
D43 74163
E31 74163
E43 74163
LOAD
CNTR
EN P
EN T
CLK
CAR
A41
D55 74367
B31 74367
E55 74367
+ X CLK SH1-D16, SH3-E16
— SHIFT 52
— X SHIFT SH1-B16
+ REQ SH4-D16
+ X2 SH3-G16
+ MEM ADDR Ø 20
+ MEM ADDR 1 21
+ MEM ADDR 2 22
+ MEM ADDR 3 23
+ MEM ADDR 4 24
+ MEM ADDR 5 25
+ MEM ADDR 6 26
+ MEM ADDR 7 27
+ MEM ADDR 8 28
+ MEM ADDR 9 29
+ MEM ADDR 10 30
+ MEM ADDR 11 31
+ MEM ADDR 12 32
+ MEM ADDR 13 33
+ MEM ADDR 14 34
+ MEM ADDR 15 35
SH1-F5 + MEM ADDR Ø
SH1-F5 + MEM ADDR 1
SH1-F5 + MEM ADDR 2
SH1-G5 + MEM ADDR 3
SH1-G5 + MEM ADDR 4
SH1-G5 + MEM ADDR 5
SH1-G5 + MEM ADDR 6
SH1-J5 + MEM ADDR 7
SH1-J5 + MEM ADDR 8
SH1-J5 + MEM ADDR 9
SH1-K5 + MEM ADDR 10
SH1-K5 + MEM ADDR 11
SH1-L5 + MEM ADDR 12
SH1-L5 + MEM ADDR 13
SH1-L5 + MEM ADDR 14
SH1-H5 + MEM ADDR 15
SH1-H5 + MEM ADDR 15

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

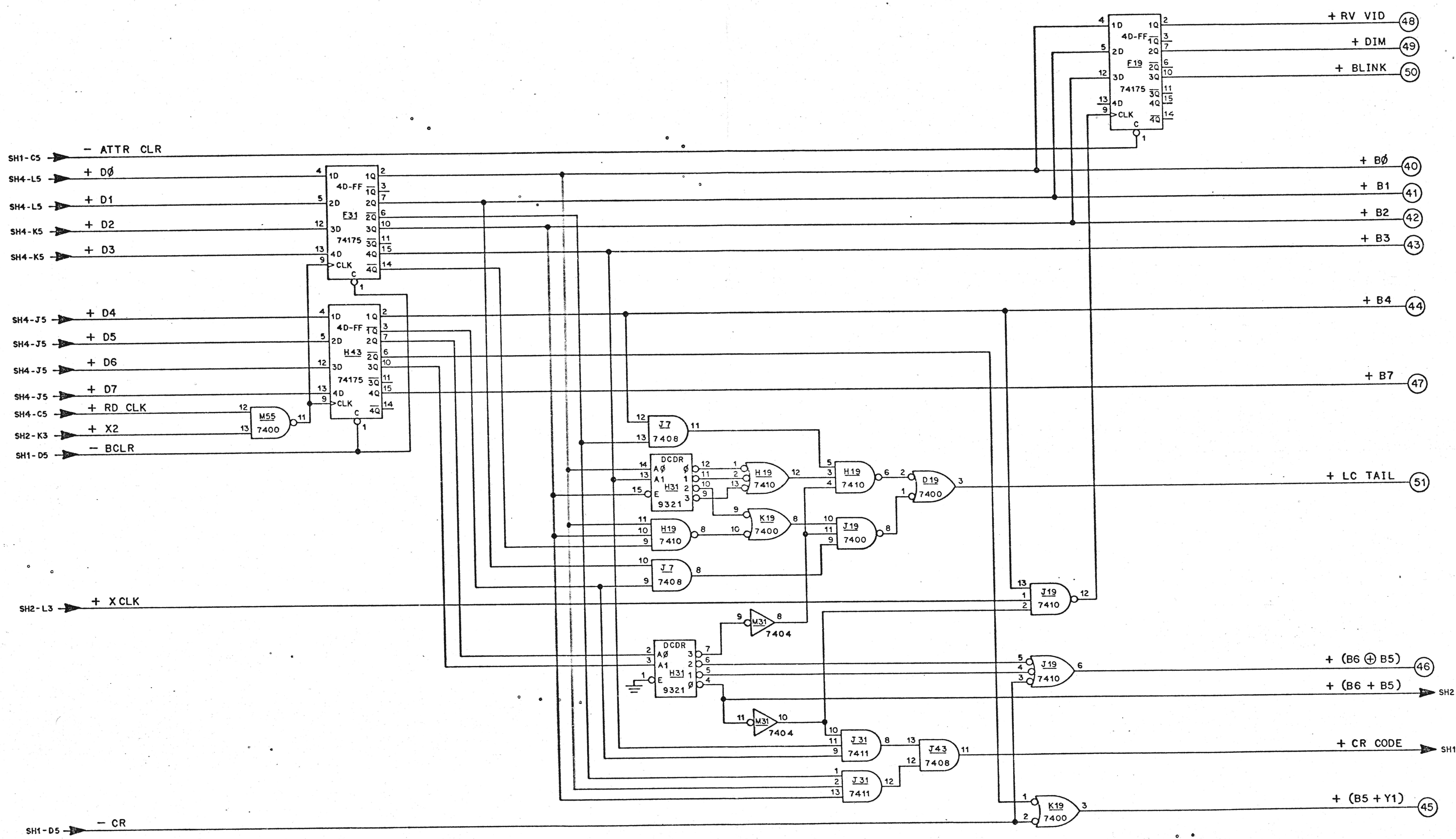
PW ASSY, TV DMA

3200

C 7549 B 7548 A 7541

8-16-76

1 4 2 9



SH1-C5 − ATTR CLR
SH4-L5 + D0
SH4-L5 + D1
SH4-K5 + D2
SH4-K5 + D3
SH4-J5 + D4
SH4-J5 + D5
SH4-J5 + D6
SH4-J5 + D7
SH4-C5 + RD CLK
SH2-K3 + X2
SH1-D5 − BCLR
SH2-L3 + XCLK
SH1-D5 − CR
4D-FF F31 74175
4D-FF H43 74175
4D-FF F19 74175
M55 7400
J7 7408
DCDR H31 9321
H19 7410
D19 7400
K19 7400
J19 7400
J19 7410
M31 7404
J31 7411
J43 7408
K19 7400
+ RV VID 48
+ DIM 49
+ BLINK 50
+ B0 40
+ B1 41
+ B2 42
+ B3 43
+ B4 44
+ B7 47
+ LC TAIL 51
+ (B6 ⊕ B5) 46
+ (B6 + B5) SH2-J16
+ CR CODE SH1-E16
+ (B5 + Y1) 45

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, TV DMA

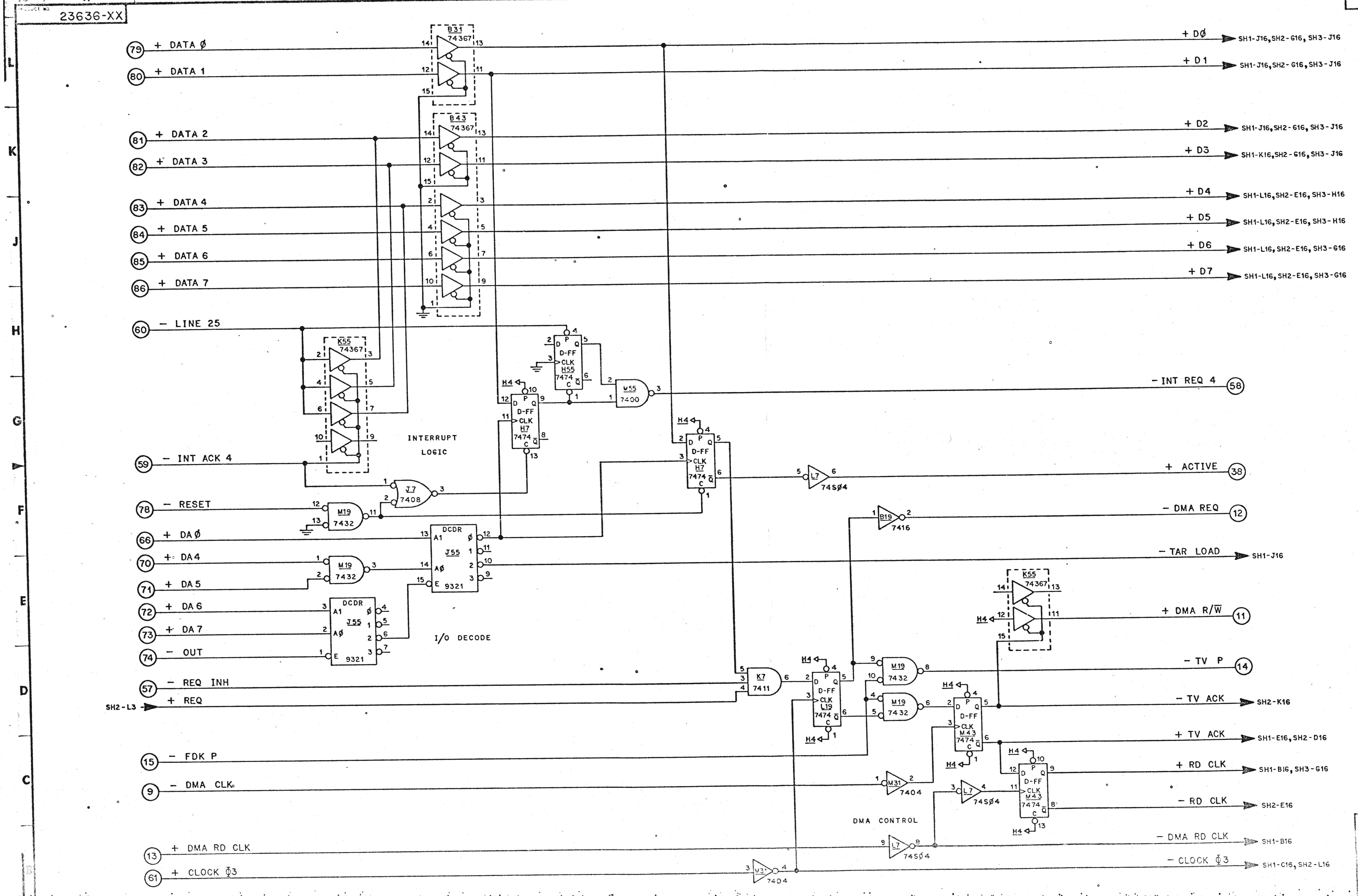
3200

C 7640 1-13-77 B 7548 A

8-17-76

1 4 3 9

23636-XX


79 + DATA Ø
80 + DATA 1
81 + DATA 2
82 + DATA 3
83 + DATA 4
84 + DATA 5
85 + DATA 6
86 + DATA 7
60 − LINE 25
59 − INT ACK 4
78 − RESET
66 + DA Ø
70 + DA4
71 + DA5
72 + DA6
73 + DA7
74 − OUT
57 − REQ INH
SH2-L3 + REQ
15 − FDK P
9 − DMA CLK
13 + DMA RD CLK
61 + CLOCK Φ3
B31 74367
B43 74367
K55 74367
H55 D-FF 7474
H7 D-FF 7474
M55 7400
J7 7408
M19 7432
J55 DCDR 9321
K7 7411
L19 D-FF 7474
L7 74SØ4
B19 7416
M43 D-FF 7474
M31 7404
H4
INTERRUPT LOGIC
I/O DECODE
DMA CONTROL
+ DØ SH1-J16, SH2-G16, SH3-J16
+ D1 SH1-J16, SH2-G16, SH3-J16
+ D2 SH1-J16, SH2-G16, SH3-J16
+ D3 SH1-K16, SH2-G16, SH3-J16
+ D4 SH1-L16, SH2-E16, SH3-H16
+ D5 SH1-L16, SH2-E16, SH3-H16
+ D6 SH1-L16, SH2-E16, SH3-G16
+ D7 SH1-L16, SH2-E16, SH3-G16
− INT REQ 4 58
+ ACTIVE 38
− DMA REQ 12
− TAR LOAD SH1-J16
+ DMA R/W̅ 11
− TV P 14
− TV ACK SH2-K16
+ TV ACK SH1-E16, SH2-D16
+ RD CLK SH1-B16, SH3-G16
− RD CLK SH2-E16
− DMA RD CLK SH1-B16
− CLOCK Φ3 SH1-C16, SH2-L16

SCHEMATIC DIAGRAM

Diablo Systems Incorpora

PW ASSY, TV DMA

3200

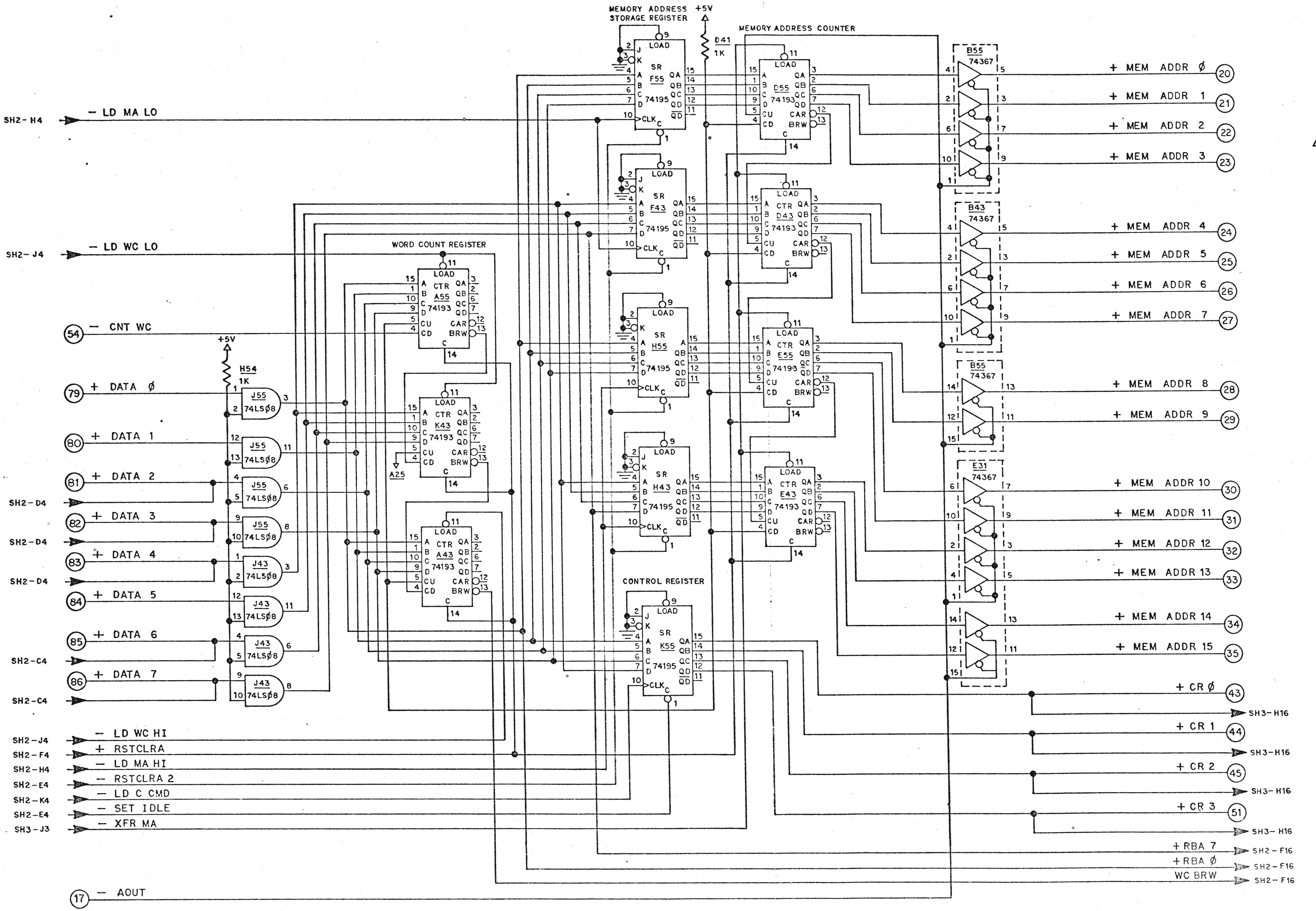
C 7540 1-13-77 B 7548 1-29-76 A 7540 8-19-76

1 4 4 9

23636-X

22

23406-XX


MEMORY ADDRESS STORAGE REGISTER
MEMORY ADDRESS COUNTER
WORD COUNT REGISTER
CONTROL REGISTER
SR F55 74195
SR F43 74195
SR H55 74195
SR H43 74195
SR K55 74195
CTR D55 74193
CTR D43 74193
CTR E55 74193
CTR E43 74193
CTR A55 74193
CTR K43 74193
CTR A43 74193
D41 1K
H54 1K
A25
J55 74LS08
J43 74LS08
B55 74367
B43 74367
E31 74367
SH2-H4 − LD MA LO
SH2-J4 − LD WC LO
54 − CNT WC
79 + DATA 0
80 + DATA 1
81 + DATA 2
82 + DATA 3
83 + DATA 4
84 + DATA 5
85 + DATA 6
86 + DATA 7
SH2-D4
SH2-C4
SH2-J4 − LD WC HI
SH2-F4 + RSTCLRA
SH2-H4 − LD MA HI
SH2-E4 − RSTCLRA 2
SH2-K4 − LD C CMD
SH2-E4 − SET IDLE
SH3-J3 − XFR MA
17 − AOUT
+ MEM ADDR 0 20
+ MEM ADDR 1 21
+ MEM ADDR 2 22
+ MEM ADDR 3 23
+ MEM ADDR 4 24
+ MEM ADDR 5 25
+ MEM ADDR 6 26
+ MEM ADDR 7 27
+ MEM ADDR 8 28
+ MEM ADDR 9 29
+ MEM ADDR 10 30
+ MEM ADDR 11 31
+ MEM ADDR 12 32
+ MEM ADDR 13 33
+ MEM ADDR 14 34
+ MEM ADDR 15 35
+ CR 0 43 SH3-H16
+ CR 1 44 SH3-H16
+ CR 2 45 SH3-H16
+ CR 3 51 SH3-H16
+ RBA 7 SH2-F16
+ RBA 0 SH2-F16
WC BRW SH2-F16
+5V

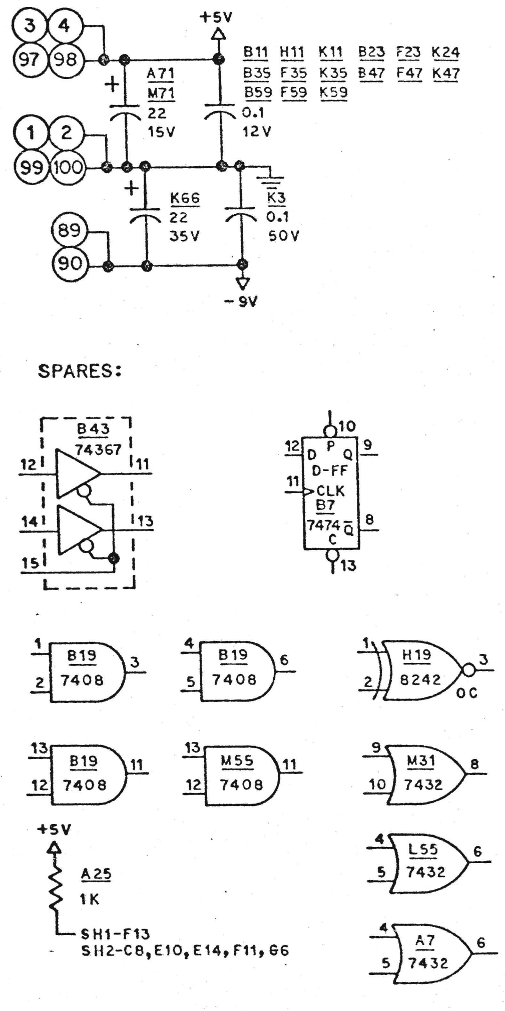
NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ±5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.

⚠5 JUMPERS SET CONTROLLER NUMBER CODE. IF ONLY ONE CONTROLLER IS USED ON SAME INTERRUPT LEVEL, LEAVE ALL INTACT.

FOR CONTROLLER	REMOVE JUMPER
2	A
3	B
4	C

23406-01 SHOWN.


+5V
B11 H11 K11 B23 F23 K24
B35 F35 K35 B47 F47 K47
B59 F59 K59
A71 M71 22 15V
0.1 12V
K66 22 35V
K3 0.1 50V
-9V
SPARES:
B43 74367
D-FF B7 7474
B19 7408
H19 8242
M55 7408
M31 7432
L55 7432
A7 7432
A25 1K
SH1-F13
SH2-C8, E10, E14, F11, G6

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE PW ASSY, RG FCA

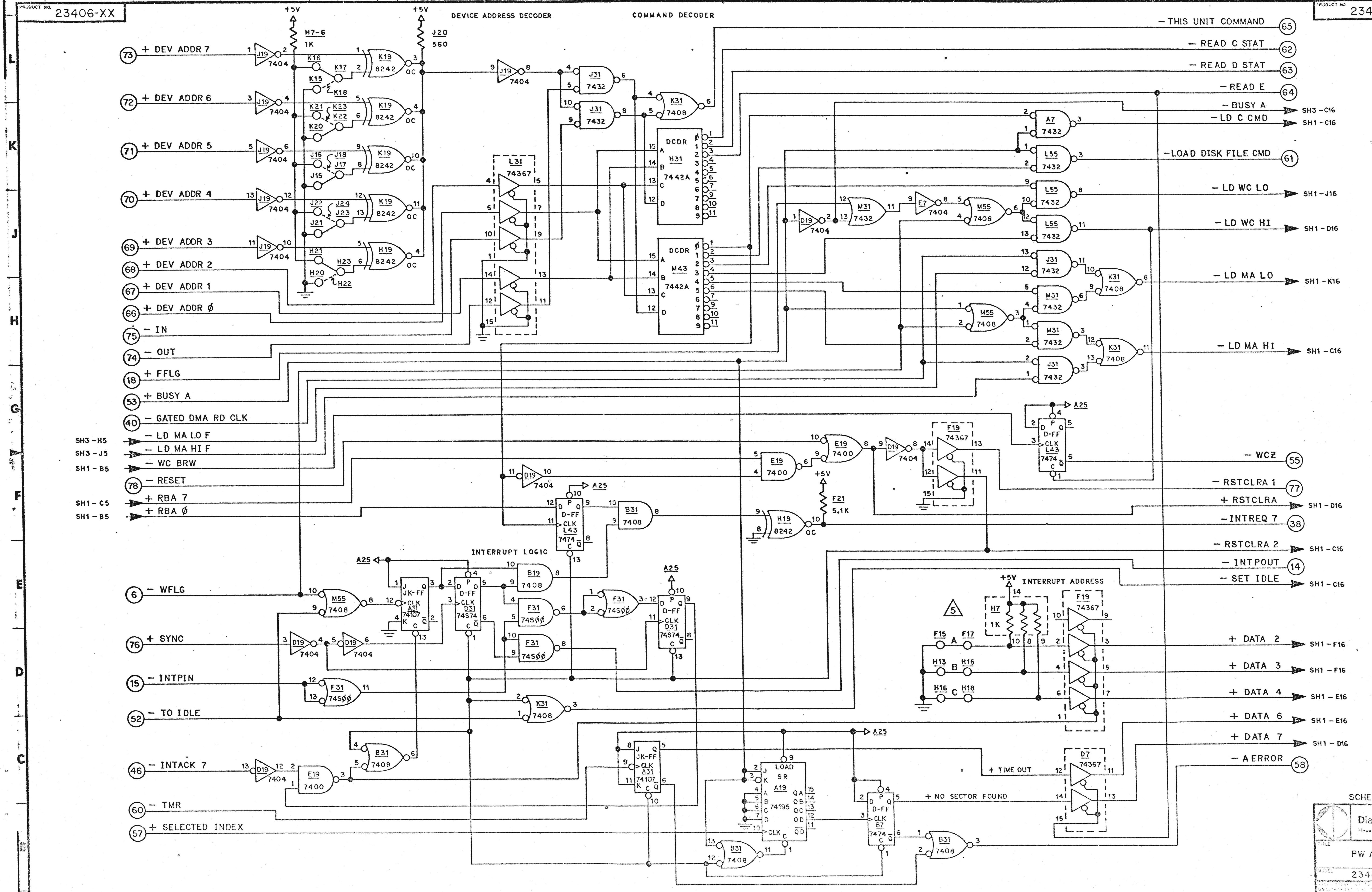
MODEL 23400

SCHEMATIC INCLUDES SHEETS 1 THRU 3

SHEET 1 TOTAL SHEETS 10

PRODUCT NO 23406-XX

A 7461


23406-XX
DEVICE ADDRESS DECODER
COMMAND DECODER
INTERRUPT LOGIC
INTERRUPT ADDRESS
+5V
H7-6 1K
J20 560
(73) + DEV ADDR 7
(72) + DEV ADDR 6
(71) + DEV ADDR 5
(70) + DEV ADDR 4
(69) + DEV ADDR 3
(68) + DEV ADDR 2
(67) + DEV ADDR 1
(66) + DEV ADDR Ø
(75) − IN
(74) − OUT
(18) + FFLG
(53) + BUSY A
(40) − GATED DMA RD CLK
SH3 - H5 − LD MA LO F
SH3 - J5 − LD MA HI F
SH1 - B5 − WC BRW
(78) − RESET
SH1 - C5 + RBA 7
SH1 - B5 + RBA Ø
(6) − WFLG
(76) + SYNC
(15) − INTPIN
(52) − TO IDLE
(46) − INTACK 7
(60) − TMR
(57) + SELECTED INDEX
− THIS UNIT COMMAND (65)
− READ C STAT (62)
− READ D STAT (63)
− READ E (64)
− BUSY A SH3 - C16
− LD C CMD SH1 - C16
− LOAD DISK FILE CMD (61)
− LD WC LO SH1 - J16
− LD WC HI SH1 - D16
− LD MA LO SH1 - K16
− LD MA HI SH1 - C16
− WCZ (55)
− RSTCLRA 1 (77)
+ RSTCLRA SH1 - D16
− INTREQ 7 (38)
− RSTCLRA 2 SH1 - C16
− INTPOUT (14)
− SET IDLE SH1 - C16
+ DATA 2 SH1 - F16
+ DATA 3 SH1 - F16
+ DATA 4 SH1 - E16
+ DATA 6 SH1 - E16
+ DATA 7 SH1 - D16
− A ERROR (58)
+ TIME OUT
+ NO SECTOR FOUND
J19 7404
K19 8242
H19 8242
K16 K17 K15 K18 K21 K23 K22 K20 J16 J18 J17 J15 J22 J24 J23 J21 H21 H23 H20 H22
L31 74367
J31 7432
K31 7408
DCDR H31 7442A
DCDR M43 7442A
A7 7432
L55 7432
M31 7432
E7 7404
M55 7408
D19 7404
J31 7432
M31 7432
K31 7408
E19 7400
F19 74367
L43 7474 D-FF
F21 5.1K
B31 7408
M55 7408
A31 74107 JK-FF
D31 74S74 D-FF
B19 7408
F31 74SØØ
A25
H7 1K
F15 A F17
H13 B H15
H16 C H18
D7 74367
A19 74195 LOAD SR
B7 7474 D-FF
5
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2
L K J H G F E D C

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE PW ASSY, RGFCA

MODEL 23400

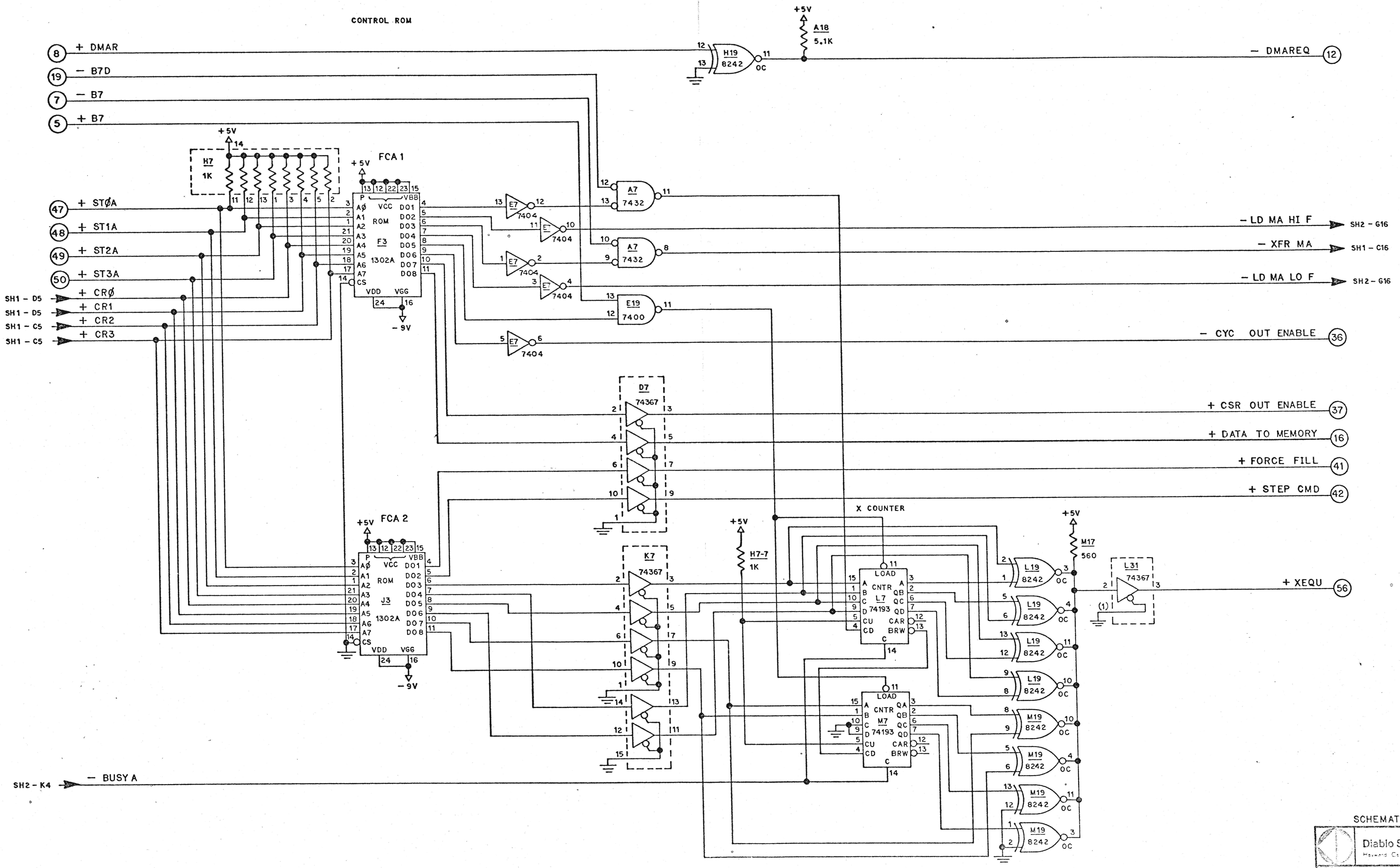
SCHEMATIC INCLUDES SHEETS 1 THRU 3 | SHEET 2 | TOTAL SHEETS 10

PRODUCT NO. 23406-XX

A 7461

7-2-75

24


CONTROL ROM
+ DMAR
- B7D
- B7
+ B7
H19 8242 OC
A18 5.1K
+5V
- DMAREQ
H7 1K
FCA 1
ROM F3 1302A
+ STØA
+ ST1A
+ ST2A
+ ST3A
SH1 - D5 + CRØ
SH1 - D5 + CR1
SH1 - C5 + CR2
SH1 - C5 + CR3
-9V
E7 7404
A7 7432
E19 7400
- LD MA HI F SH2 - G16
- XFR MA SH1 - C16
- LD MA LO F SH2 - G16
- CYC OUT ENABLE
D7 74367
+ CSR OUT ENABLE
+ DATA TO MEMORY
+ FORCE FILL
+ STEP CMD
FCA 2
ROM J3 1302A
K7 74367
X COUNTER
H7-7 1K
LOAD CNTR L7 74193
LOAD CNTR M7 74193
L19 8242 OC
M19 8242 OC
M17 560
L31 74367
+ XEQU
SH2 - K4 - BUSY A

SCHEMATIC DIAGRAM

Diablo Systems Incorporate
Hayward California 94545

TITLE PW ASSY, RGFCA

MODEL 23400

ENG. R... 5/28/76
CHECKED 7-3-75

SCHEMATIC INCLUDES SHEETS 1 THRU 3

SHEET 3 TOTAL SHEETS 10

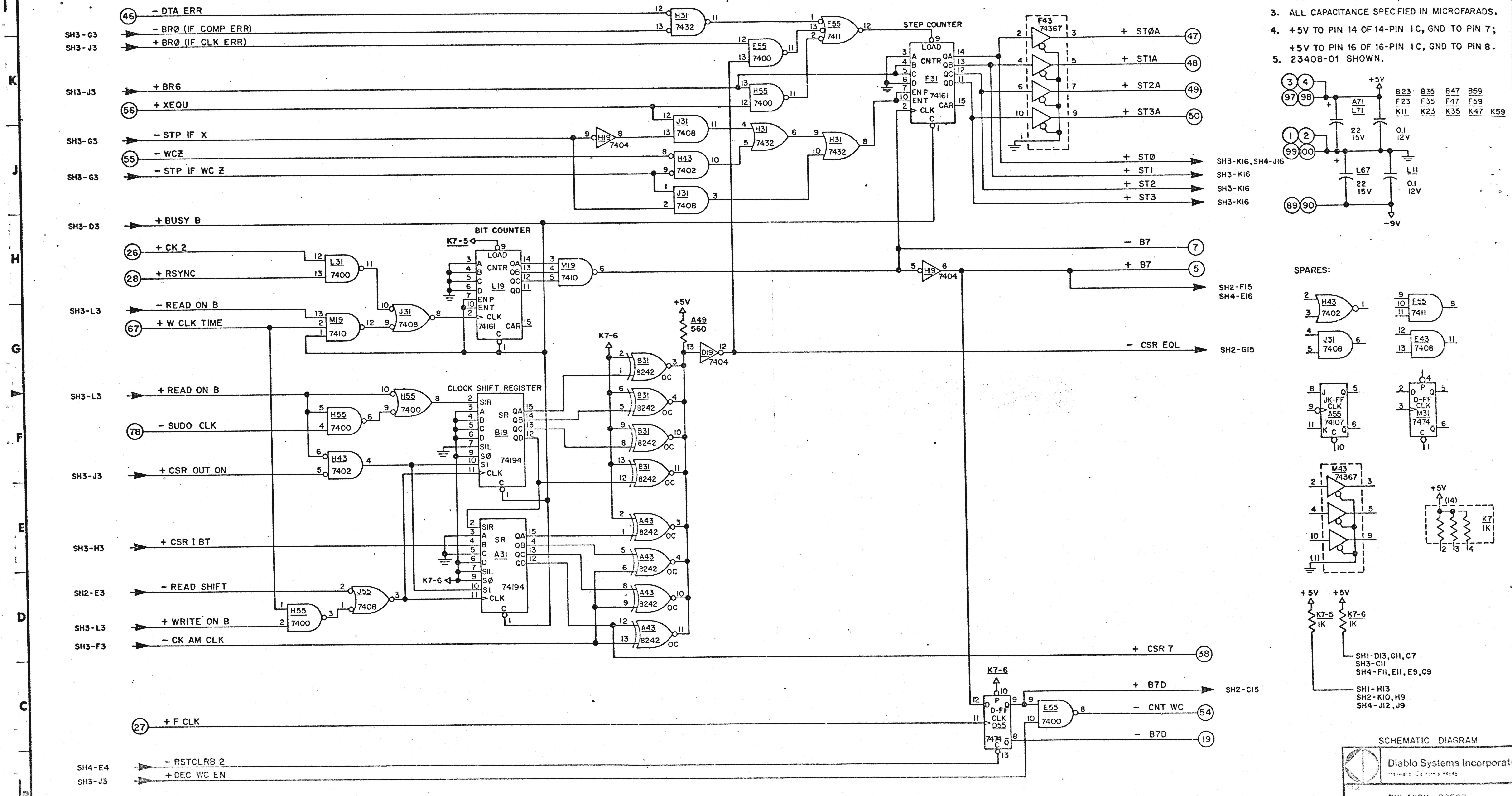
PRODUCT NO. 23406-XX

PRODUCT NO. 23408-XX

23408-XX D2

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7; +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8.
5. 23408-01 SHOWN.



46 - DTA ERR
SH3-G3 - BRØ (IF COMP ERR)
SH3-J3 + BRØ (IF CLK ERR)
SH3-J3 + BR6
56 + XEQU
SH3-G3 - STP IF X
55 - WCZ
SH3-G3 - STP IF WC Z
SH3-D3 + BUSY B
26 + CK 2
28 + RSYNC
SH3-L3 - READ ON B
67 + W CLK TIME
SH3-L3 + READ ON B
78 - SUDO CLK
SH3-J3 + CSR OUT ON
SH3-H3 + CSR I BT
SH2-E3 - READ SHIFT
SH3-L3 + WRITE ON B
SH3-F3 - CK AM CLK
27 + F CLK
SH4-E4 - RSTCLRB 2
SH3-J3 + DEC WC EN
H31 7432
F55 7411
E55 7400
H55 7400
J31 7408
H19 7404
H43 7402
STEP COUNTER
F31 74161
F43 74367
+ STØA 47
+ STIA 48
+ ST2A 49
+ ST3A 50
+ STØ SH3-K16, SH4-J16
+ STI SH3-K16
+ ST2 SH3-K16
+ ST3 SH3-K16
BIT COUNTER
K7-5
L19 74161
L31 7400
M19 7410
- B7 7
+ B7 5
SH2-F15 SH4-E16
+5V
A49 560
K7-6
D19 7404
- CSR EQL SH2-G15
CLOCK SHIFT REGISTER
B19 74194
A31 74194
B31 8242
A43 8242
J55 7408
+ CSR 7 38
D-FF D55 7474
+ B7D SH2-C15
- CNT WC 54
- B7D 19
3 4 97 98
A71 L71
22 15V
0.1 12V
B23 B35 B47 B59
F23 F35 F47 F59
K11 K23 K35 K47 K59
1 2 99 100
L67 22 15V
L11 0.1 12V
89 90
-9V
SPARES:
H43 7402
F55 7411
J31 7408
E43 7408
JK-FF A55 74107
D-FF M31 7474
M43 74367
+5V (14) K7 1K
K7-5 1K
K7-6 1K
SH1-D13, G11, C7
SH3-C11
SH4-F11, E11, E9, C9
SH1-H13
SH2-K10, H9
SH4-J12, J9

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RGFCB

23400

23408-XX

1 4

12

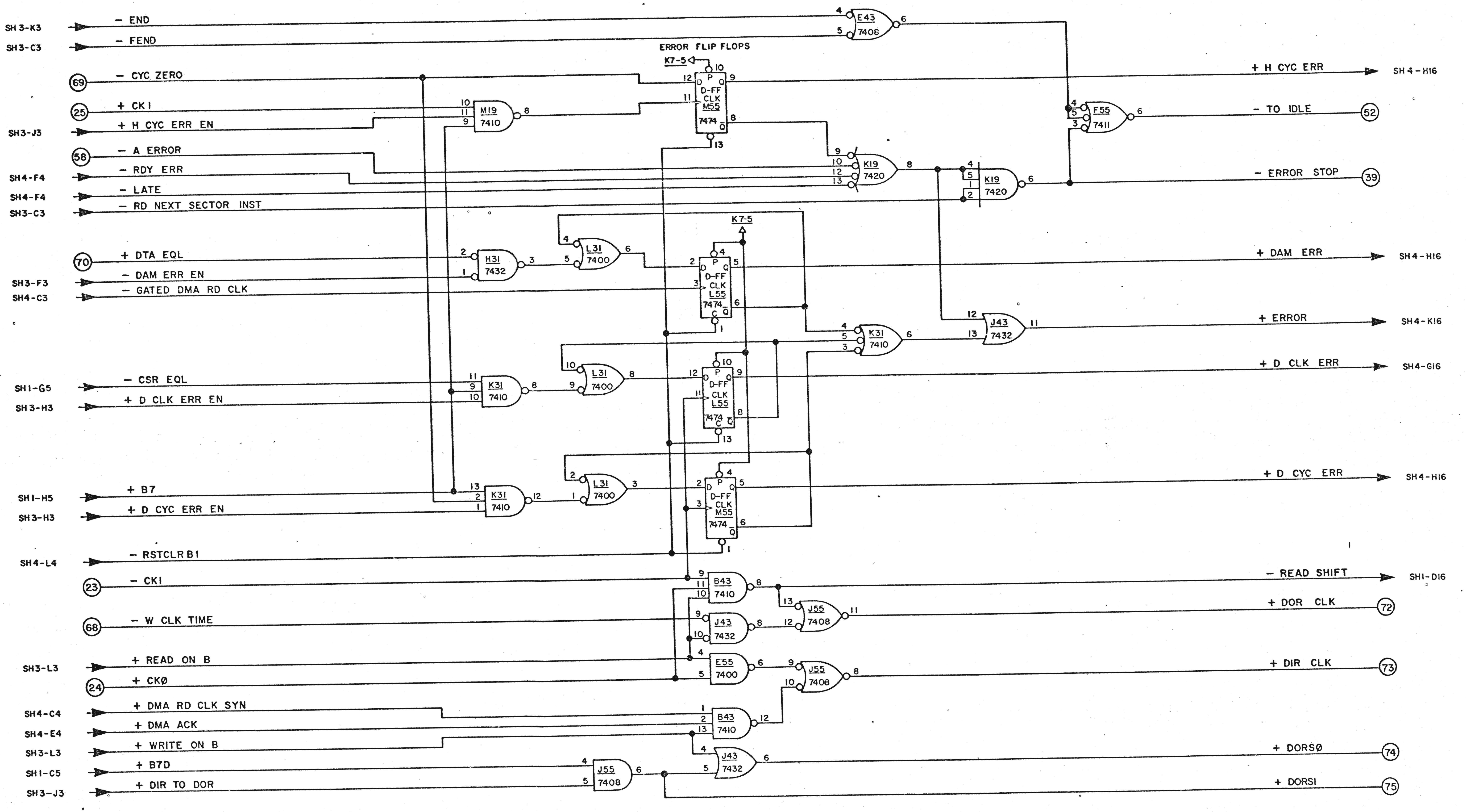
23408-XX

E ADL 1-6-75

26

PRODUCT NO. 23408-XX

PRODUCT NO. 23408-XX D2


SH3-K3
- END
SH3-C3
- FEND
E43
7408
ERROR FLIP FLOPS
K7-5
69
- CYC ZERO
D-FF
CLK
M55
7474
+ H CYC ERR
SH4-H16
25
+ CK1
M19
7410
SH3-J3
+ H CYC ERR EN
F55
7411
- TO IDLE
52
58
- A ERROR
SH4-F4
- RDY ERR
K19
7420
SH4-F4
- LATE
- ERROR STOP
39
SH3-C3
- RD NEXT SECTOR INST
K7-5
L31
7400
70
+ DTA EQL
H31
7432
+ DAM ERR
SH4-H16
SH3-F3
- DAM ERR EN
L55
SH4-C3
- GATED DMA RD CLK
+ ERROR
SH4-K16
J43
7432
K31
7410
+ D CLK ERR
SH4-G16
SH1-G5
- CSR EQL
SH3-H3
+ D CLK ERR EN
+ D CYC ERR
SH4-H16
SH1-H5
+ B7
SH3-H3
+ D CYC ERR EN
SH4-L4
- RSTCLR B1
- READ SHIFT
SH1-D16
23
- CK1
B43
7410
J55
7408
+ DOR CLK
72
68
- W CLK TIME
SH3-L3
+ READ ON B
E55
7400
+ DIR CLK
73
24
+ CKØ
SH4-C4
+ DMA RD CLK SYN
SH4-E4
+ DMA ACK
SH3-L3
+ WRITE ON B
SH1-C5
+ B7D
+ DORSØ
74
SH3-J3
+ DIR TO DOR
+ DORS1
75

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

TITLE PW ASSY, RGFCB

MODEL 23400

1 4

2 12

23408-XX

PRODUCT NO. 23408-XX

C 7623 12-14-76 | B 7573 [illegible] | A 7461 1 JUN 76

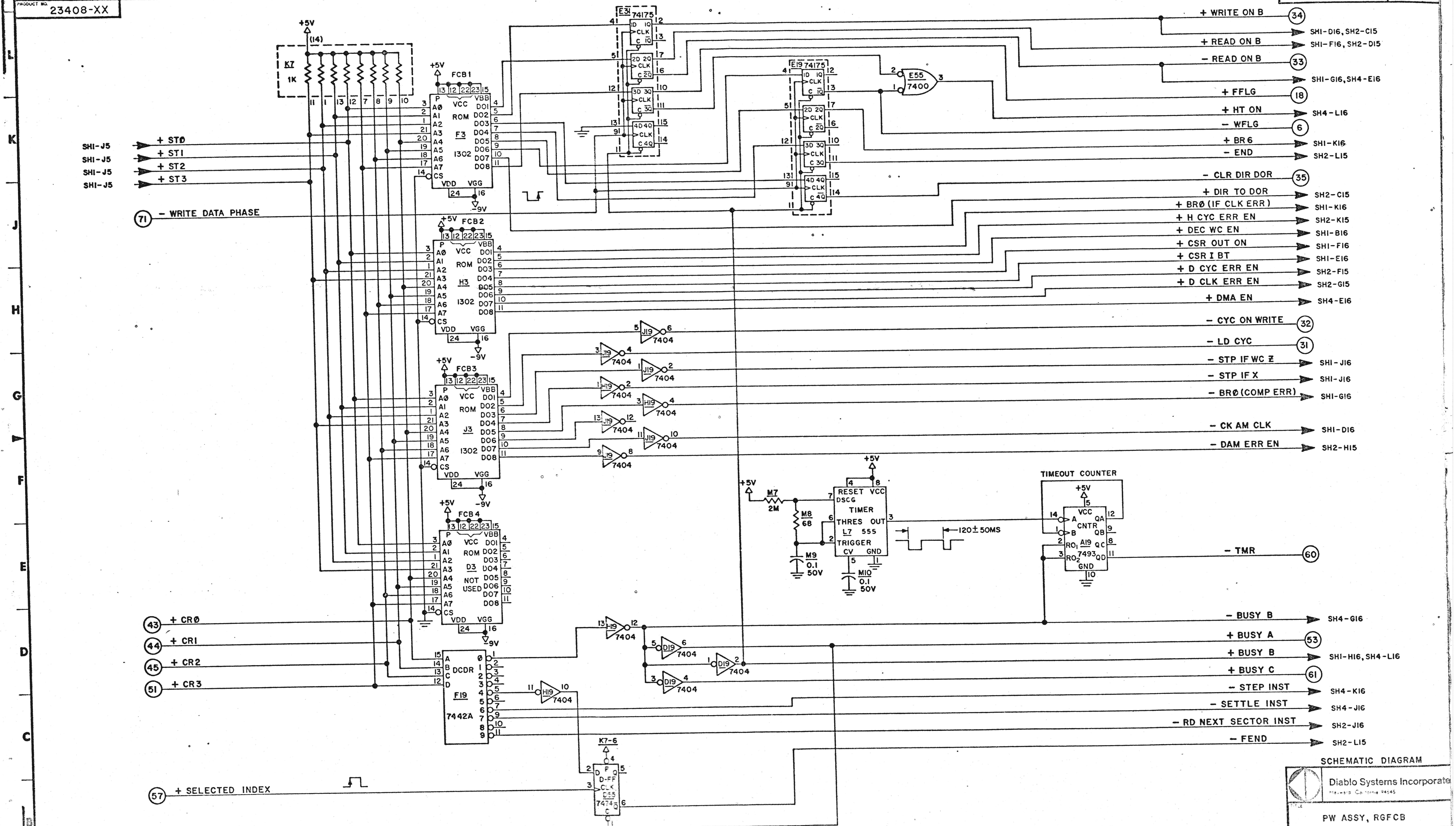
5/28/76

5/25/76

5/25/76

E. ADAMS

PRODUCT NO. 23408-XX


K7 1K
+5V
(14)
FCB1
ROM F3 1302
FCB2
ROM H3 1302
FCB3
ROM J3 1302
FCB4
ROM D3 NOT USED
VCC VBB VDD VGG
-9V
A0 A1 A2 A3 A4 A5 A6 A7 CS P
DO1 DO2 DO3 DO4 DO5 DO6 DO7 DO8
E3 74175
E19 74175
E55 7400
SH1-J5 + ST0
SH1-J5 + ST1
SH1-J5 + ST2
SH1-J5 + ST3
(71) - WRITE DATA PHASE
+ WRITE ON B (34) SH1-D16, SH2-C15
+ READ ON B SH1-F16, SH2-D15
- READ ON B (33) SH1-G16, SH4-E16
+ FFLG (18)
+ HT ON SH4-L16
- WFLG (6)
+ BR6 SH1-K16
- END SH2-L15
- CLR DIR DOR (35)
+ DIR TO DOR SH2-C15
+ BR0 (IF CLK ERR) SH1-K16
+ H CYC ERR EN SH2-K15
+ DEC WC EN SH1-B16
+ CSR OUT ON SH1-F16
+ CSR I BT SH1-E16
+ D CYC ERR EN SH2-F15
+ D CLK ERR EN SH2-G15
+ DMA EN SH4-E16
J19 7404
H19 7404
- CYC ON WRITE (32)
- LD CYC (31)
- STP IF WC Z SH1-J16
- STP IF X SH1-J16
- BR0 (COMP ERR) SH1-G16
- CK AM CLK SH1-D16
- DAM ERR EN SH2-H15
+5V M7 2M
M8 68
M9 0.1 50V
M10 0.1 50V
RESET VCC DSCG TIMER THRES OUT L7 555 TRIGGER CV GND
120 ± 50MS
TIMEOUT COUNTER
VCC CNTR A19 7493 QA QB QC QD RO1 RO2 GND
- TMR (60)
(43) + CR0
(44) + CR1
(45) + CR2
(51) + CR3
DCDR F19 7442A
D19 7404
- BUSY B SH4-G16
+ BUSY A (53)
+ BUSY B SH1-H16, SH4-L16
+ BUSY C (61)
- STEP INST SH4-K16
- SETTLE INST SH4-J16
- RD NEXT SECTOR INST SH2-J16
- FEND SH2-L15
K7-6
D-FF D55 7474
(57) + SELECTED INDEX

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

PW ASSY, RGFCB

23400

23408-XX

D2

3 12

1 4

C 7623 12-14-76

B 7573

A 7461

5/28/76

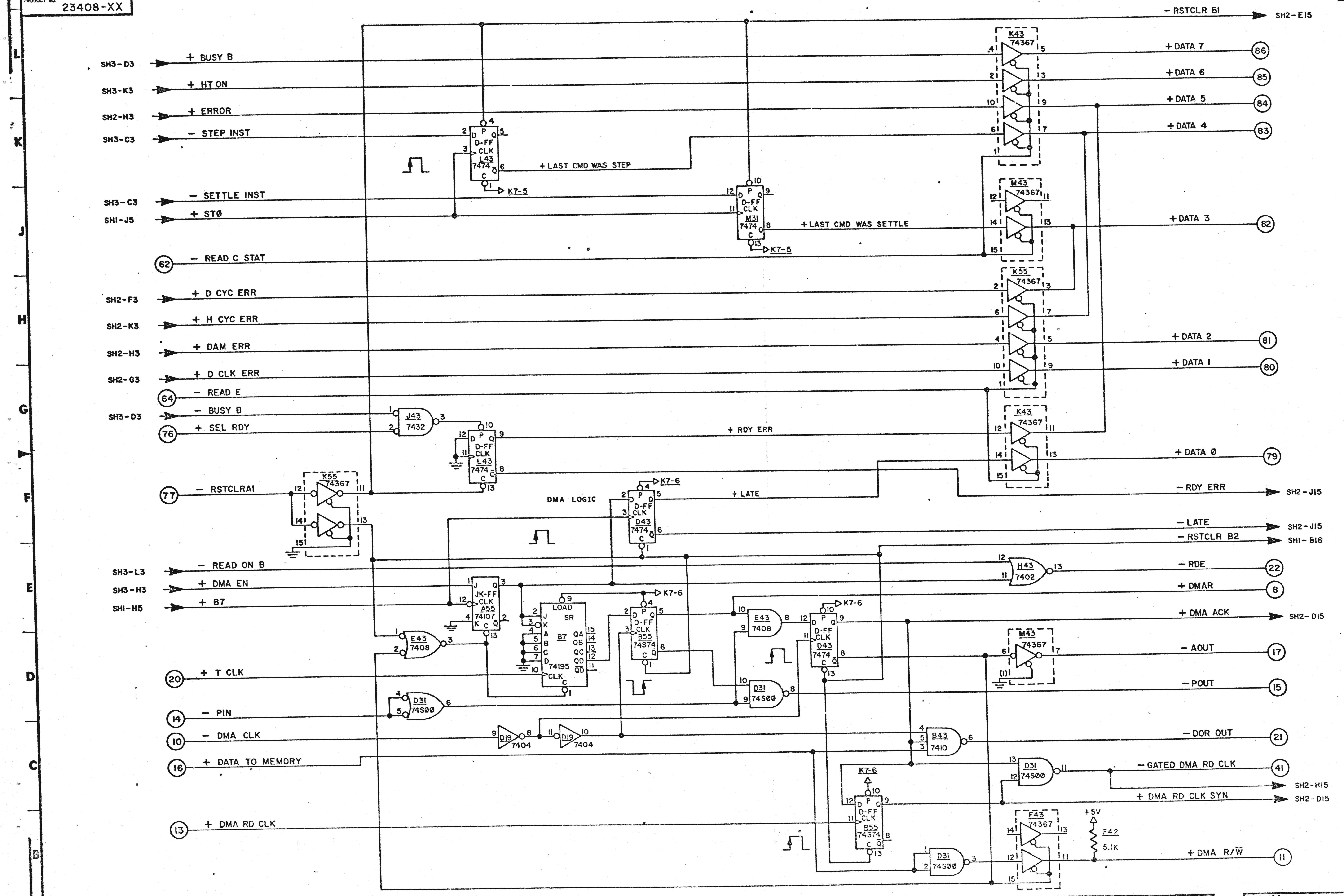
5/28/76

5/28/76

E. ADAMS

28

23408-XX



- RSTCLR B1
SH2-E15
+ BUSY B
+ HT ON
+ ERROR
- STEP INST
- SETTLE INST
+ STØ
- READ C STAT
+ D CYC ERR
+ H CYC ERR
+ DAM ERR
+ D CLK ERR
- READ E
- BUSY B
+ SEL RDY
- RSTCLRA1
- READ ON B
+ DMA EN
+ B7
+ T CLK
- PIN
- DMA CLK
+ DATA TO MEMORY
+ DMA RD CLK
SH3-D3
SH3-K3
SH2-H3
SH3-C3
SH1-J5
SH2-F3
SH2-K3
SH2-G3
SH3-L3
SH3-H3
SH1-H5
L43
7474
D-FF
+ LAST CMD WAS STEP
K7-5
M31
+ LAST CMD WAS SETTLE
K43
74367
M43
K55
+ DATA 7
+ DATA 6
+ DATA 5
+ DATA 4
+ DATA 3
+ DATA 2
+ DATA 1
+ DATA Ø
J43
7432
+ RDY ERR
- RDY ERR
SH2-J15
DMA LOGIC
D43
K7-6
+ LATE
- LATE
- RSTCLR B2
SH1-B16
H43
7402
- RDE
+ DMAR
+ DMA ACK
SH2-D15
A55
JK-FF
74107
B7
74195
LOAD
SR
B55
74S74
E43
7408
D31
74S00
- AOUT
- POUT
D19
7404
B43
7410
- DOR OUT
- GATED DMA RD CLK
SH2-H15
+ DMA RD CLK SYN
F43
+5V
F42
5.1K
+ DMA R/W̄
86
85
84
83
82
81
80
79
62
64
76
77
22
8
17
15
21
41
11
20
14
10
16
13

SCHEMATIC DIAGRAM

Diablo Systems Incorporate
Hayward, California 94545

TITLE
PW ASSY, RGFCB

MODEL
23400

PROPRIETARY INFORMATION
UNAUTHORIZED DISCLOSURE
OR USE PROHIBITED

SYSTEM LOGIC NO.

SHEET | TOTAL SHEETS | SIZE
4 | 12 | D

PRODUCT NO.
23408-XX

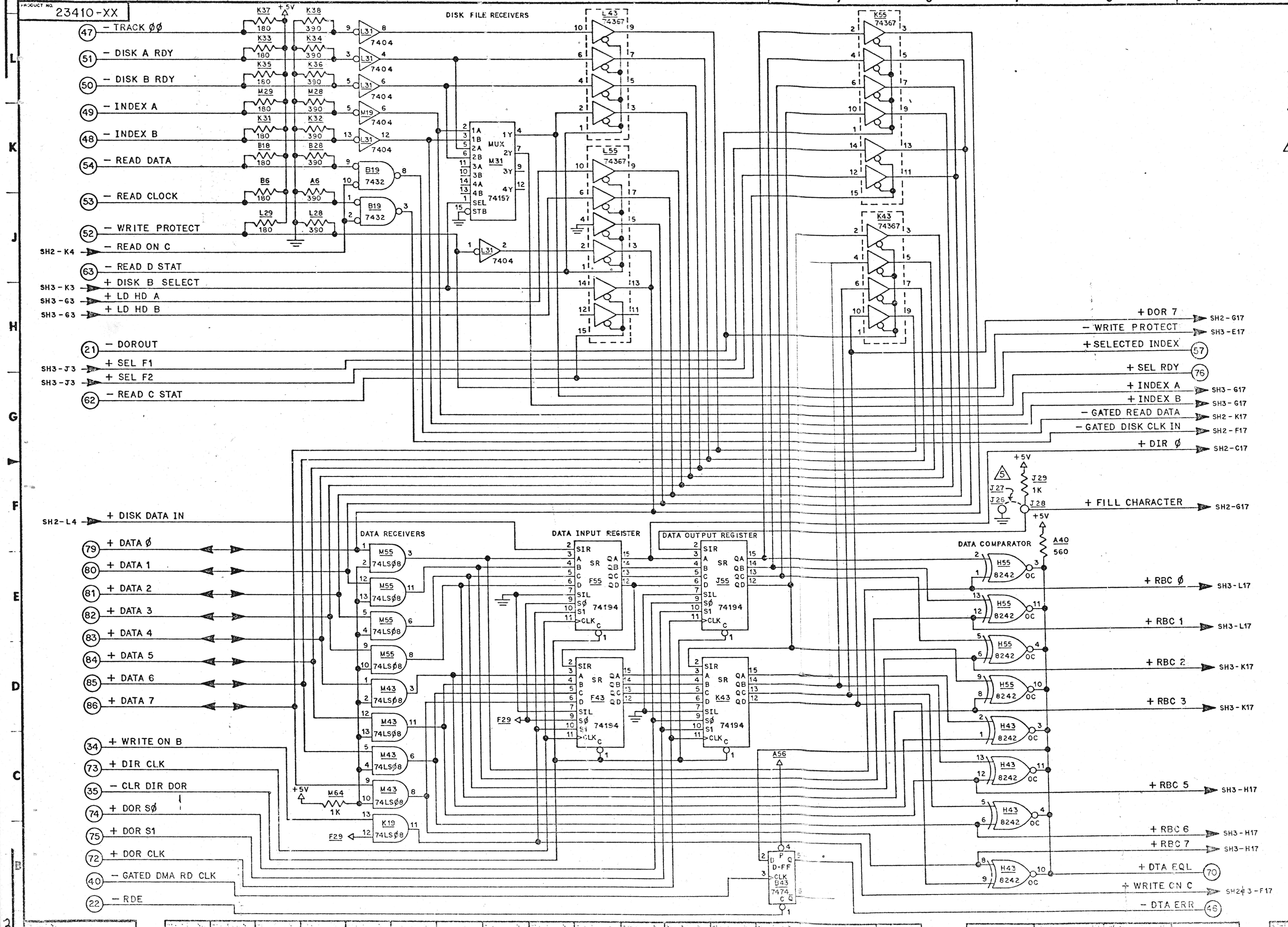
SCHEMATIC INCLUDES SHEETS 1 THRU 4

REV	ECO NO.	REV	ECO NO.	REV	ECO NO.
C	7623 12-14-76	B	7573 3-20-76	A	7461 1 JUN 76

5/28/76
Kluen 5/28/76
CHECKED F. Dunlap 5/29/76
E. ADAMS 5/28/76

PRODUCT NO. 23408-XX

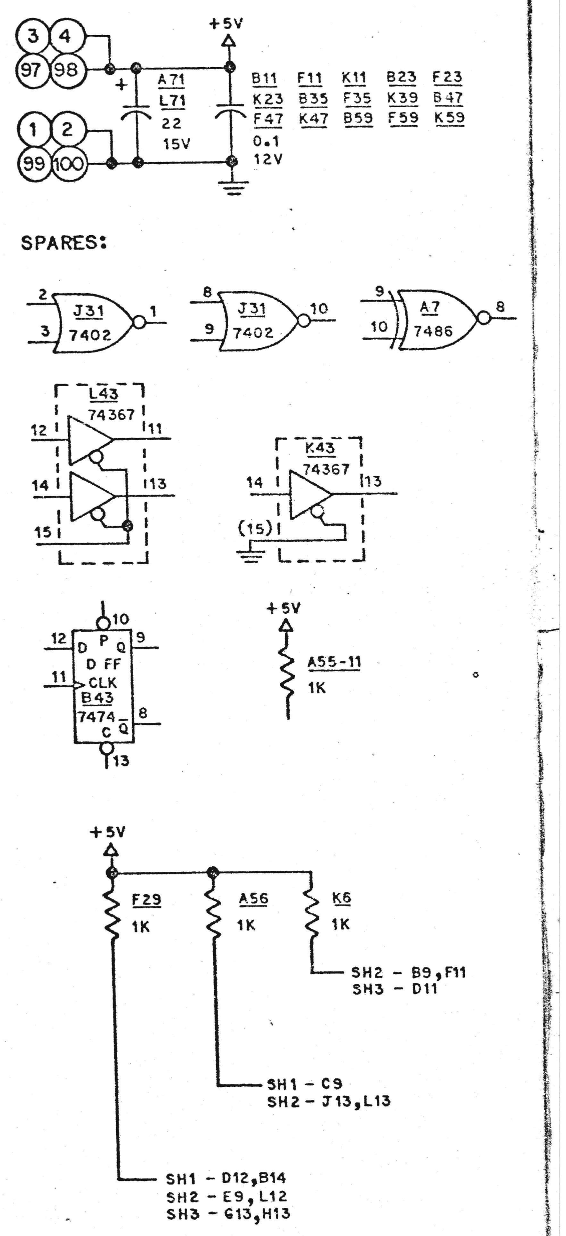
29


DISK FILE RECEIVERS
− TRACK 00
− DISK A RDY
− DISK B RDY
− INDEX A
− INDEX B
− READ DATA
− READ CLOCK
− WRITE PROTECT
SH2-K4 − READ ON C
− READ D STAT
SH3-K3 + DISK B SELECT
SH3-G3 + LD HD A
SH3-G3 + LD HD B
− DOROUT
SH3-J3 + SEL F1
SH3-J3 + SEL F2
− READ C STAT
SH2-L4 + DISK DATA IN
+ DATA 0
+ DATA 1
+ DATA 2
+ DATA 3
+ DATA 4
+ DATA 5
+ DATA 6
+ DATA 7
+ WRITE ON B
+ DIR CLK
− CLR DIR DOR
+ DOR S0
+ DOR S1
+ DOR CLK
− GATED DMA RD CLK
− RDE
47
51
50
49
48
54
53
52
63
21
62
79
80
81
82
83
84
85
86
34
73
35
74
75
72
40
22
K37 180
K38 390
K33 180
K34 390
K35 180
K36 390
M29 180
M28 390
K31 180
K32 390
B18 180
B28 390
B6 180
A6 390
L29 180
L28 390
+5V
L31 7404
M19 7404
B19 7432
M31 74157 MUX
1A 1B 2A 2B 3A 3B 4A 4B SEL STB 1Y 2Y 3Y 4Y
L43 74367
L55 74367
K55 74367
K43 74367
+ DOR 7 SH2-G17
− WRITE PROTECT SH3-E17
+ SELECTED INDEX 57
+ SEL RDY 76
+ INDEX A SH3-G17
+ INDEX B SH3-G17
− GATED READ DATA SH2-K17
− GATED DISK CLK IN SH2-F17
+ DIR 0 SH2-C17
+5V
J29 1K
J27
J26
J28
5
+ FILL CHARACTER SH2-G17
DATA RECEIVERS
M55 74LS08
M43 74LS08
K19 74LS08
M64 1K
F29
DATA INPUT REGISTER
F55 74194
F43 74194
SIR A B C D SIL S0 S1 CLK SR QA QB QC QD
DATA OUTPUT REGISTER
J55 74194
K43 74194
A56
B43 7474 D-FF
DATA COMPARATOR
A40 560
H55 8242 OC
H43 8242 OC
+ RBC 0 SH3-L17
+ RBC 1 SH3-L17
+ RBC 2 SH3-K17
+ RBC 3 SH3-K17
+ RBC 5 SH3-H17
+ RBC 6 SH3-H17
+ RBC 7 SH3-H17
+ DTA EQL 70
+ WRITE ON C SH2&3-F17
− DTA ERR 46

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
4. +5V TO PIN 14 OF 14-PIN IC, GND TO PIN 7;
   +5V TO PIN 16 OF 16-PIN IC, GND TO PIN 8;
   +5V TO PIN 8 OF 8-PIN IC, GND TO PIN 4.

⚠5 ON 23410-01 FILL CHARACTER IS "FF" WITHOUT JUMPER.
ON 23410-02 FILL CHARACTER IS "0" WITH JUMPER.


3
4
97
98
1
2
99
100
+5V
A71
L71
22
15V
B11 F11 K11 B23 F23
K23 B35 F35 K39 B47
F47 K47 B59 F59 K59
0.1
12V
SPARES:
J31 7402
J31 7402
A7 7486
L43 74367
K43 74367
(15)
B43 7474 D FF
+5V
A55-11 1K
+5V
F29 1K
A56 1K
K6 1K
SH2 - B9, F11
SH3 - D11
SH1 - C9
SH2 - J13, L13
SH1 - D12, B14
SH2 - E9, L12
SH3 - G13, H13

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

TITLE PW ASSY, RGFCC

MODEL 23400

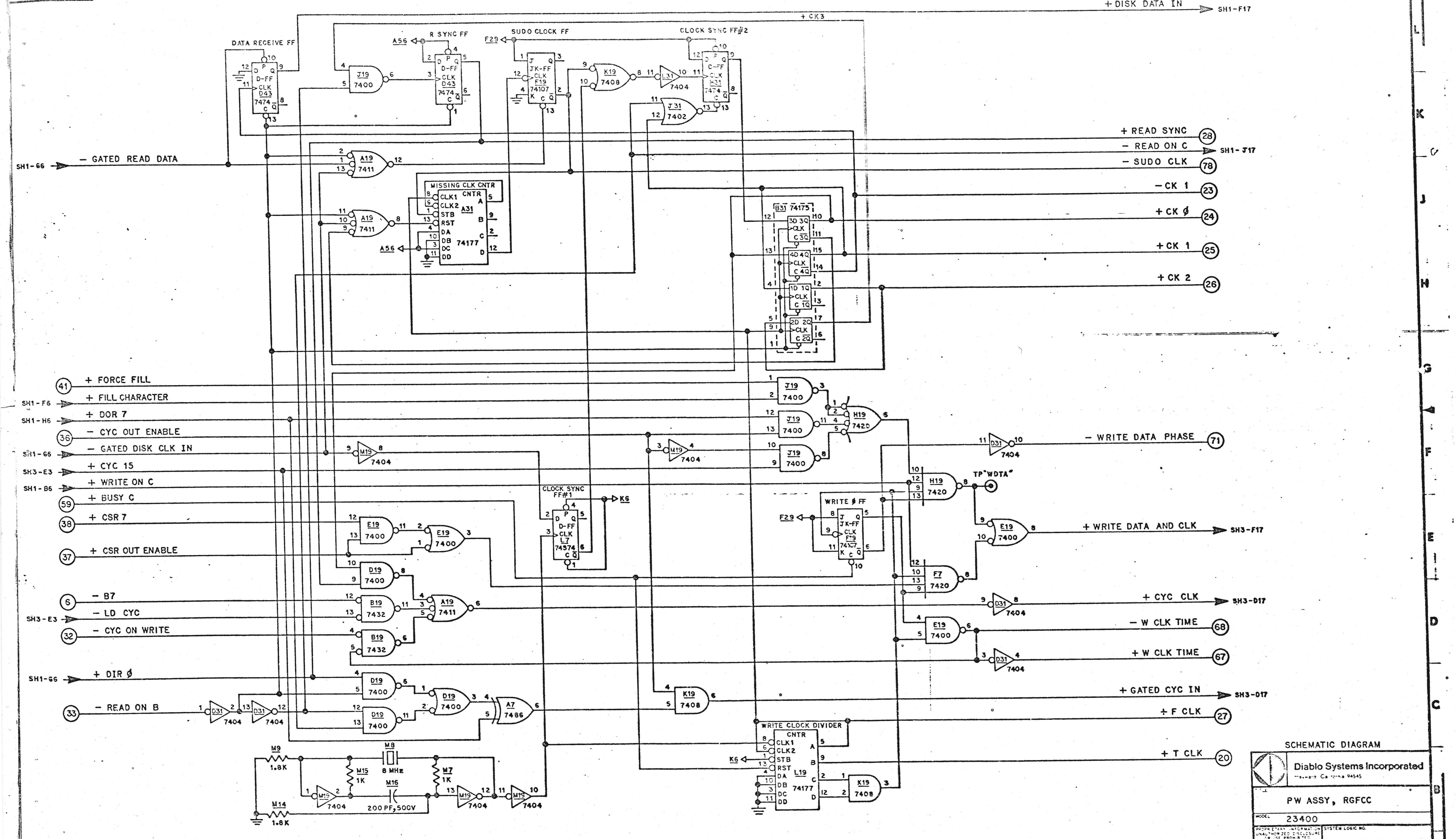
SCHEMATIC INCLUDES SHEETS 1 THRU 3

SHEET 1 TOTAL SHEETS 11 D

PRODUCT NO 23410-XX

A 7461

2-12-76


+ DISK DATA IN
SH1-F17
+ CK3
DATA RECEIVE FF
D-FF
D43
7474
R SYNC FF
A56
J19
7400
SUDO CLOCK FF
F29
JK-FF
F19
74107
K19
7408
L31
7404
CLOCK SYNC FF#2
J31
7402
+ READ SYNC
28
− READ ON C
SH1-J17
− SUDO CLK
78
SH1-G6
− GATED READ DATA
A19
7411
MISSING CLK CNTR
A31
74177
− CK 1
23
+ CK Ø
24
B31 74175
+ CK 1
25
+ CK 2
26
41
+ FORCE FILL
SH1-F6
+ FILL CHARACTER
SH1-H6
+ DOR 7
36
− CYC OUT ENABLE
SH1-G6
− GATED DISK CLK IN
M19
7404
SH3-E3
+ CYC 15
SH1-B6
+ WRITE ON C
59
+ BUSY C
38
+ CSR 7
37
+ CSR OUT ENABLE
H19
7420
− WRITE DATA PHASE
71
D31
TP "WDTA"
CLOCK SYNC FF#1
L7
74S74
K6
WRITE Ø FF
+ WRITE DATA AND CLK
SH3-F17
E19
7400
D19
F7
7420
6
− B7
SH3-E3
− LD CYC
32
− CYC ON WRITE
B19
7432
+ CYC CLK
SH3-D17
− W CLK TIME
68
+ W CLK TIME
67
SH1-G6
+ DIR Ø
33
− READ ON B
A7
7486
+ GATED CYC IN
SH3-D17
+ F CLK
27
WRITE CLOCK DIVIDER
L19
74177
+ T CLK
20
M9
1.8K
M15
1K
M8
8 MHz
M16
200 PF, 500V
M7
1K
M14
1.8K

SCHEMATIC DIAGRAM

Diablo Systems Incorporated
Hayward, California 94545

TITLE PW ASSY, RGFCC

MODEL 23400

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO.

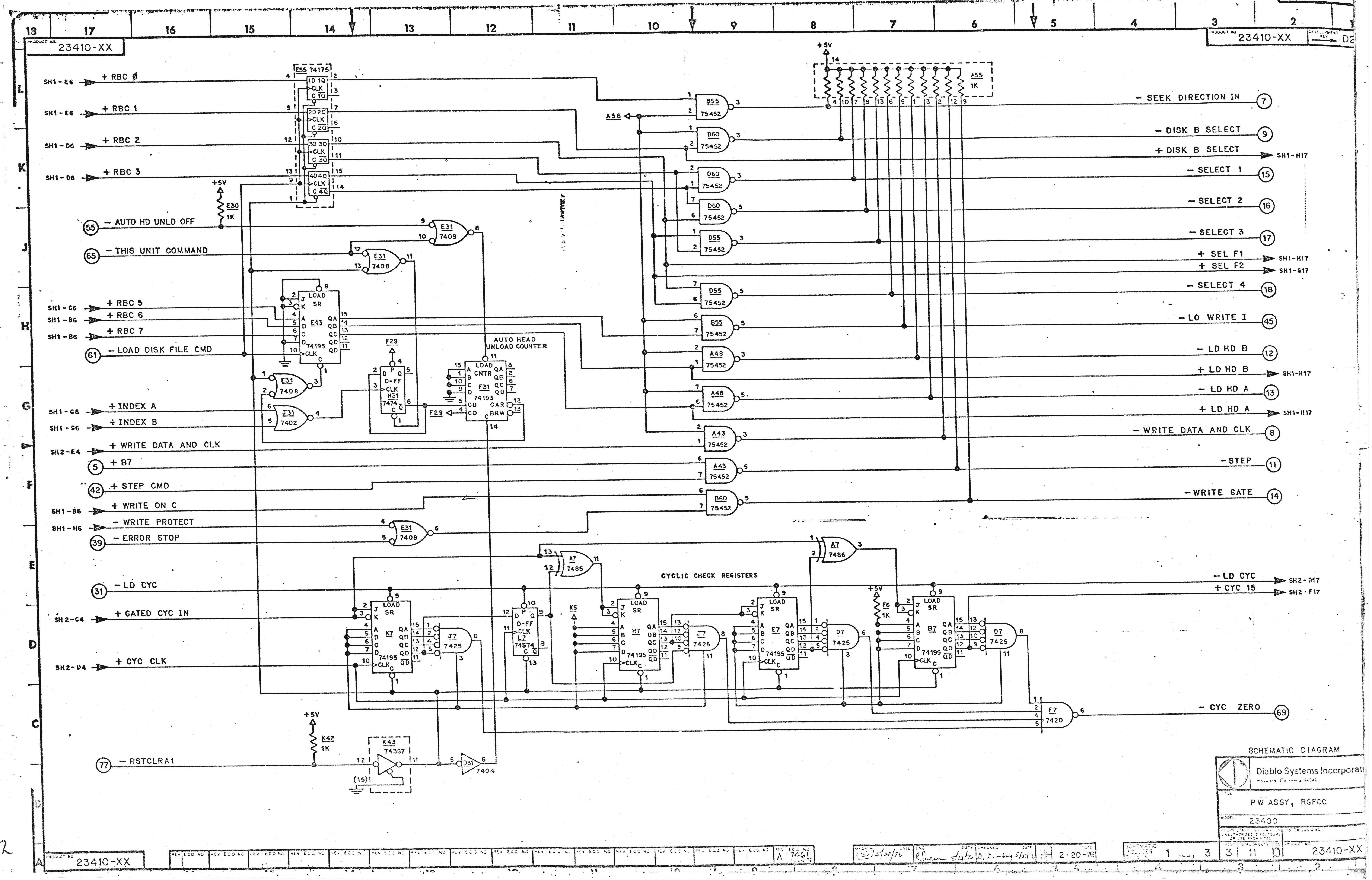
5/28/76 K Sum 5/22/76 CHECKED L. Zanko 5/27/76 DRAWN HNC DATE 2-18-76

SCHEMATIC INCLUDES SHEETS 1 THRU 3

SHEET 2 TOTAL SHEETS 11 SIZE D

PRODUCT NO. 23410-XX REV A

A 7461


23410-XX
SH1-E6 + RBC 0
SH1-E6 + RBC 1
SH1-D6 + RBC 2
SH1-D6 + RBC 3
E55 74175
+5V
E30 1K
55 - AUTO HD UNLD OFF
E31 7408
65 - THIS UNIT COMMAND
SH1-C6 + RBC 5
SH1-B6 + RBC 6
SH1-B6 + RBC 7
61 - LOAD DISK FILE CMD
E43 74195
LOAD SR
F29
H31 7474 D-FF
AUTO HEAD UNLOAD COUNTER
F31 74193
E31 7408
SH1-G6 + INDEX A
SH1-G6 + INDEX B
J31 7402
F29
SH2-E4 + WRITE DATA AND CLK
5 + B7
42 + STEP CMD
SH1-B6 + WRITE ON C
SH1-H6 - WRITE PROTECT
39 - ERROR STOP
E31 7408
A56
B55 75452
B60 75452
D60 75452
D55 75452
A48 75452
A43 75452
A55 1K
- SEEK DIRECTION IN 7
- DISK B SELECT 9
+ DISK B SELECT SH1-H17
- SELECT 1 15
- SELECT 2 16
- SELECT 3 17
+ SEL F1 SH1-H17
+ SEL F2 SH1-G17
- SELECT 4 18
- LO WRITE I 45
- LD HD B 12
+ LD HD B SH1-H17
- LD HD A 13
+ LD HD A SH1-H17
- WRITE DATA AND CLK 8
- STEP 11
- WRITE GATE 14
A7 7486
CYCLIC CHECK REGISTERS
31 - LD CYC
SH2-C4 + GATED CYC IN
SH2-D4 + CYC CLK
K7 74195
J7 7425
L7 74S74 D-FF
K5
H7 74195
J7 7425
E7 74195
D7 7425
F6 1K
B7 74195
D7 7425
- LD CYC SH2-D17
+ CYC 15 SH2-F17
F7 7420
- CYC ZERO 69
77 - RSTCLRA1
K42 1K
K43 74367
(15)
D31 7404

SCHEMATIC DIAGRAM

Diablo Systems Incorporat
Hayward, California 94545

TITLE PW ASSY, RGFCC

MODEL 23400

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

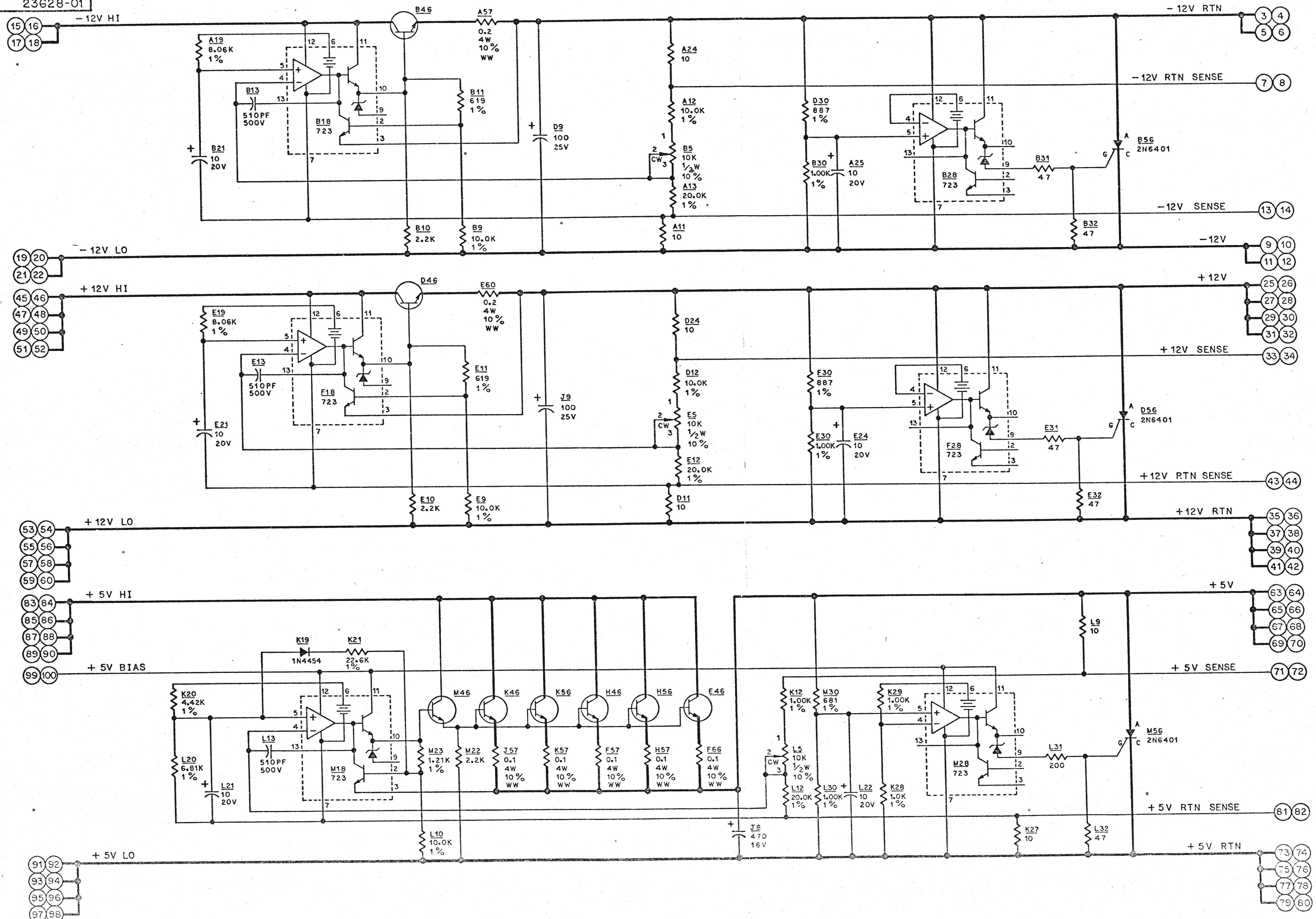
MFG DATE	ENG DATE	CHECKED DATE	REV DATE	SCHEMATIC INCLUDES SHEETS	SHEET	TOTAL SHEETS	SIZE	PRODUCT NO
5/28/76	5/28/76	5/27/76	N/C 2-20-76	1 THRU 3	3	11	D	23410-XX

REV A 7461

32

23628-01

23628-01 → D4


17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2
L K J H G F E D C
−12V HI
15 16 17 18
A19 8.06K 1%
B13 510PF 500V
B18 723
B21 10 20V
B46
A57 0.2 4W 10% WW
B11 619 1%
B10 2.2K
B9 10.0K 1%
D9 100 25V
A24 10
A12 10.0K 1%
B5 10K 1/2W 10%
CW
A13 20.0K 1%
A11 10
D30 887 1%
B30 1.00K 1%
A25 10 20V
B28 723
B31 47
B32 47
B56 2N6401
A G C
−12V RTN
3 4 5 6
−12V RTN SENSE
7 8
−12V SENSE
13 14
−12V
9 10 11 12
−12V LO
19 20 21 22
+12V HI
45 46 47 48 49 50 51 52
E19 8.06K 1%
E13 510PF 500V
F18 723
E21 10 20V
D46
E60 0.2 4W 10% WW
E11 619 1%
E10 2.2K
E9 10.0K 1%
J9 100 25V
D24 10
D12 10.0K 1%
E5 10K 1/2W 10%
E12 20.0K 1%
D11 10
F30 887 1%
E30 1.00K 1%
E24 10 20V
F28 723
E31 47
E32 47
D56 2N6401
+12V
25 26 27 28 29 30 31 32
+12V SENSE
33 34
+12V RTN SENSE
43 44
+12V RTN
35 36 37 38 39 40 41 42
+12V LO
53 54 55 56 57 58 59 60
+5V HI
83 84 85 86 87 88 89 90
+5V BIAS
99 100
K19 1N4454
K21 22.6K 1%
K20 4.42K 1%
L20 6.81K 1%
L21 10 20V
L13 510PF 500V
M18 723
M46
K46
K56
H46
H56
E46
M23 1.21K 1%
M22 2.2K
J57 0.1 4W 10% WW
K57 0.1 4W 10% WW
F57 0.1 4W 10% WW
H57 0.1 4W 10% WW
F66 0.1 4W 10% WW
L10 10.0K 1%
J6 470 16V
K12 1.00K 1%
M30 681 1%
K29 1.00K 1%
L5 10K 1/2W 10%
L12 20.0K 1%
L30 1.00K 1%
L22 10 20V
K28 1.0K 1%
M28 723
L31 200
L32 47
K27 10
L9 10
M56 2N6401
+5V
63 64 65 66 67 68 69 70
+5V SENSE
71 72
+5V RTN SENSE
81 82
+5V RTN
73 74 75 76 77 78 79 80
+5V LO
91 92 93 94 95 96 97 98

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%
3. ALL 1% RESISTORS ARE 1/8 WATT.
4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
5. ALL TRANSISTORS ARE TIP3055 OR MJE 3055K.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG 12/5

3200

33

23628-01

A 7555 9/24/76

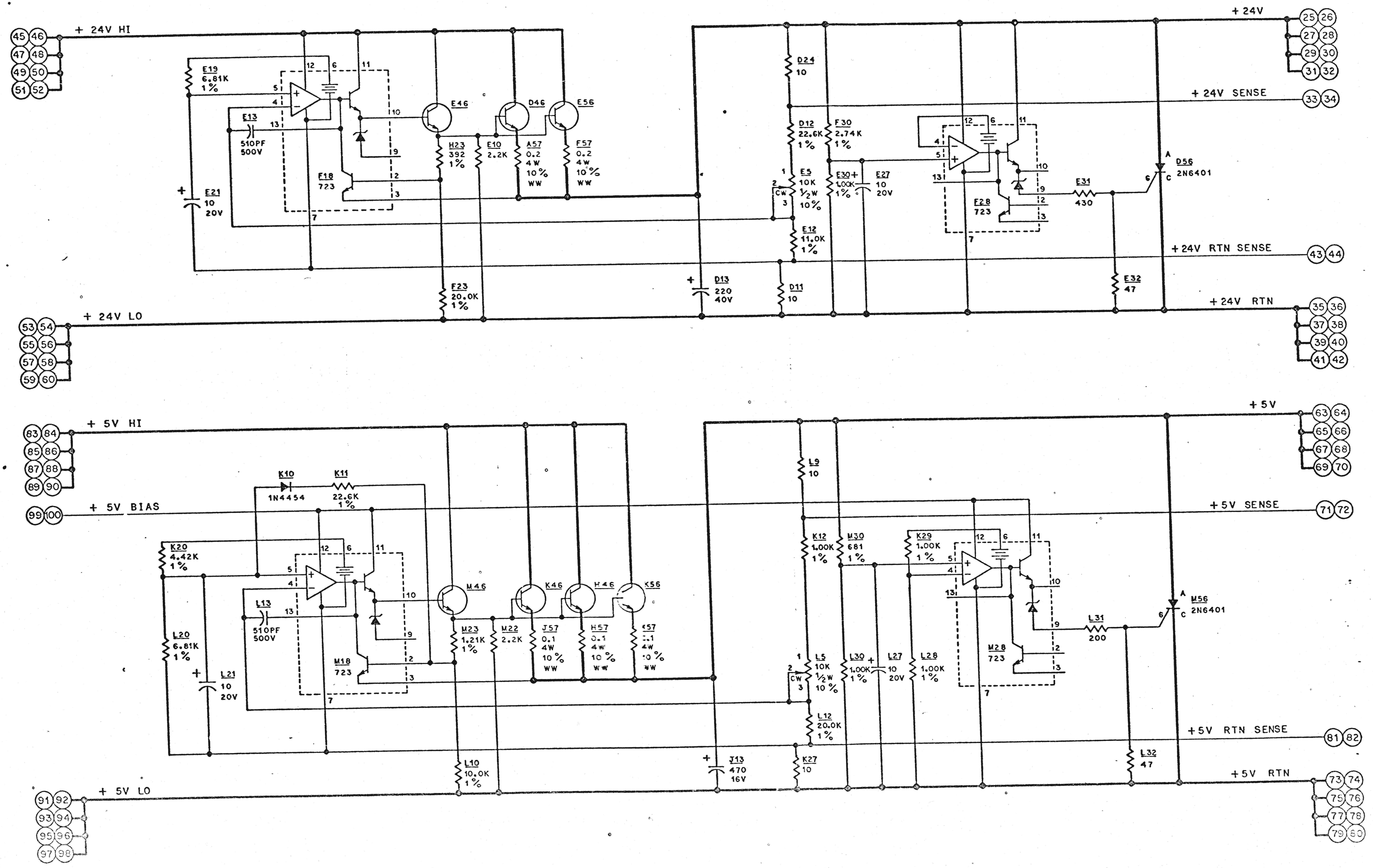
9/24/76 9/24/76 9/24/76

8-26-76

1 1 1 7

23628-01

23626-01



+ 24V HI
45 46 47 48 49 50 51 52
E19 6.81K 1%
E13 510PF 500V
E21 10 20V
F18 723
E46
D46
E56
H23 392 1%
E10 2.2K
A57 0.2 4W 10% WW
F57 0.2 4W 10% WW
F23 20.0K 1%
+ 24V LO
53 54 55 56 57 58 59 60
D13 220 40V
D24 10
D12 22.6K 1%
F30 2.74K 1%
E5 10K 1/2W 10%
CW
E30 1.00K 1%
E27 10 20V
E12 11.0K 1%
D11 10
F28 723
E31 430
E32 47
D56 2N6401
+ 24V
25 26 27 28 29 30 31 32
+ 24V SENSE
33 34
+24V RTN SENSE
43 44
+24V RTN
35 36 37 38 39 40 41 42
+ 5V HI
83 84 85 86 87 88 89 90
K10 1N4454
K11 22.6K 1%
+ 5V BIAS
99 100
K20 4.42K 1%
L13 510PF 500V
L20 6.81K 1%
L21 10 20V
M18 723
M46
K46
H46
K56
M23 1.21K 1%
M22 2.2K
J57 0.1 4W 10% WW
H57 0.1 4W 10% WW
K57 0.1 4W 10% WW
L10 10.0K 1%
+ 5V LO
91 92 93 94 95 96 97 98
J13 470 16V
L9 10
K12 1.00K 1%
M30 681 1%
K29 1.00K 1%
L5 10K 1/2W 10%
L30 1.00K 1%
L27 10 20V
L28 1.00K 1%
M28 723
L12 20.0K 1%
K27 10
L31 200
L32 47
M56 2N6401
+5V
63 64 65 66 67 68 69 70
+5V SENSE
71 72
+5V RTN SENSE
81 82
+5V RTN
73 74 75 76 77 78 79 80

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ± 5%.
3. ALL 1% RESISTORS ARE 1/8 WATT.
4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
5. ALL TRANSISTORS ARE TIP3055 OR MJE 3055K.

SCHEMATIC DIAGRAM

Diablo Systems Incorpor

PW ASSY, RG 24/5

3200

9-8-76

1 1

1 7

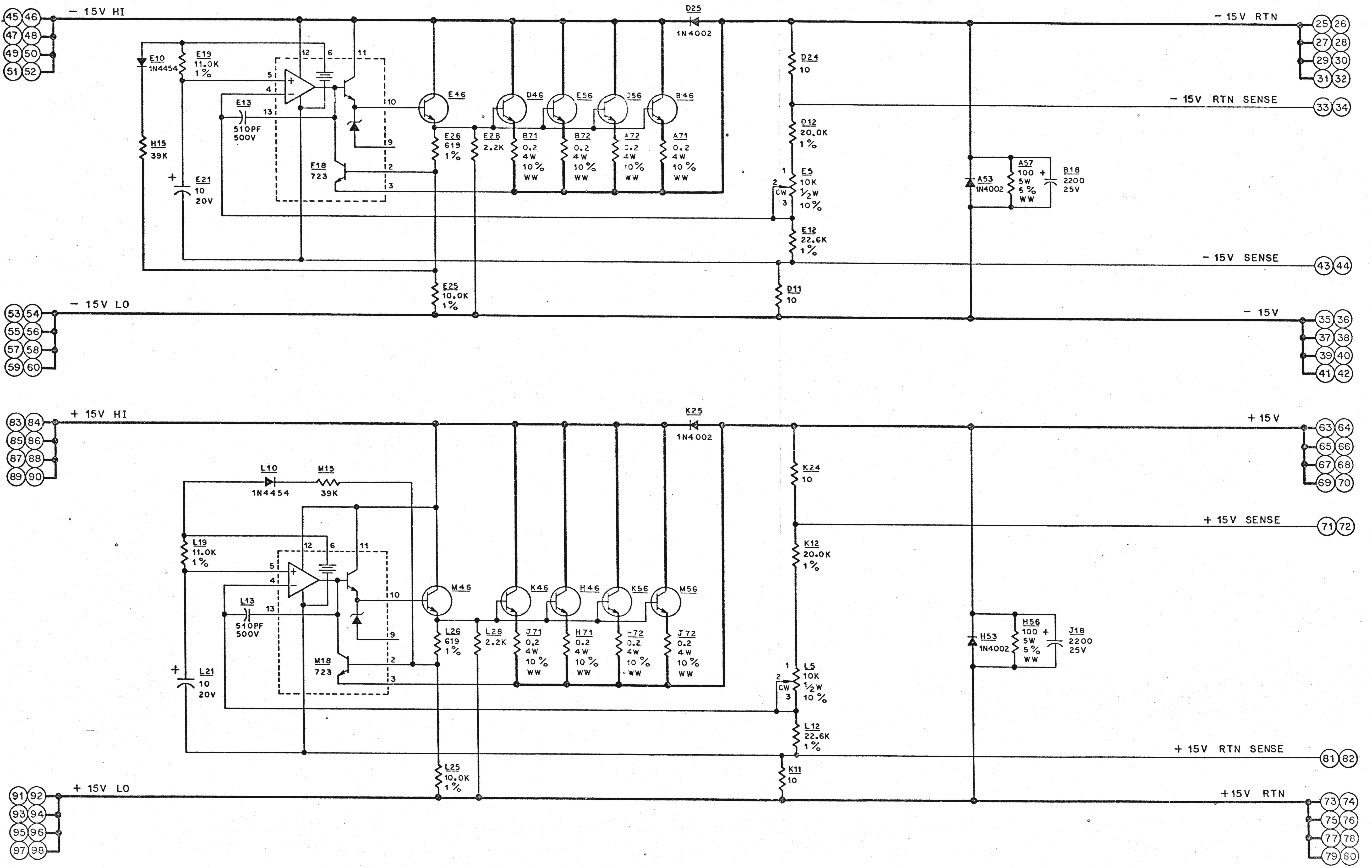
23626-01

23626

34

23624-01

23624-01 → D4



45 46 47 48 49 50 51 52
− 15V HI
D25
1N4002
− 15V RTN
25 26 27 28 29 30 31 32
E10
1N4454
E19
11.0K
1%
E13
510PF
500V
12 6 11
5 4 13 10 9 2 3
F18
723
H15
39K
E21
10
20V
E46
D46
E56
D56
B46
E26
619
1%
E28
2.2K
B71
0.2
4W
10%
WW
B72
0.2
4W
10%
WW
A72
0.2
4W
10%
WW
A71
0.2
4W
10%
WW
D24
10
− 15V RTN SENSE
33 34
D12
20.0K
1%
E5
10K
½W
10%
CW
E12
22.6K
1%
A53
1N4002
A57
100
5W
5%
WW
B18
2200
25V
− 15V SENSE
43 44
E25
10.0K
1%
D11
10
53 54 55 56 57 58 59 60
− 15V LO
− 15V
35 36 37 38 39 40 41 42
83 84 85 86 87 88 89 90
+ 15V HI
K25
1N4002
+ 15V
63 64 65 66 67 68 69 70
L10
1N4454
M15
39K
K24
10
+ 15V SENSE
71 72
L19
11.0K
1%
L13
510PF
500V
M18
723
L21
10
20V
M46
K46
H46
K56
M56
L26
619
1%
L28
2.2K
J71
0.2
4W
10%
WW
H71
0.2
4W
10%
WW
H72
0.2
4W
10%
WW
J72
0.2
4W
10%
WW
K12
20.0K
1%
L5
10K
½W
10%
CW
L12
22.6K
1%
H53
1N4002
H56
100
5W
5%
WW
J18
2200
25V
+ 15V RTN SENSE
81 82
L25
10.0K
1%
K11
10
91 92 93 94 95 96 97 98
+ 15V LO
+15V RTN
73 74 75 76 77 78 79 80

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL RESISTANCES SPECIFIED IN OHMS.
2. ALL RESISTORS ARE 1/4 WATT, ±5%.
3. ALL 1% RESISTORS ARE 1/8 WATT.
4. ALL CAPACITANCE SPECIFIED IN MICROFARADS.
5. ALL TRANSISTORS ARE TIP3055 OR MJE 3055K.

SCHEMATIC DIAGRAM

Diablo Systems Incorporated

PW ASSY, RG 15V

3200

23624-01	A 7555 9/24/76	9/21/76	9/24/76	9/24/76	N/C 9-7-76	1 1	1 6

23624-01

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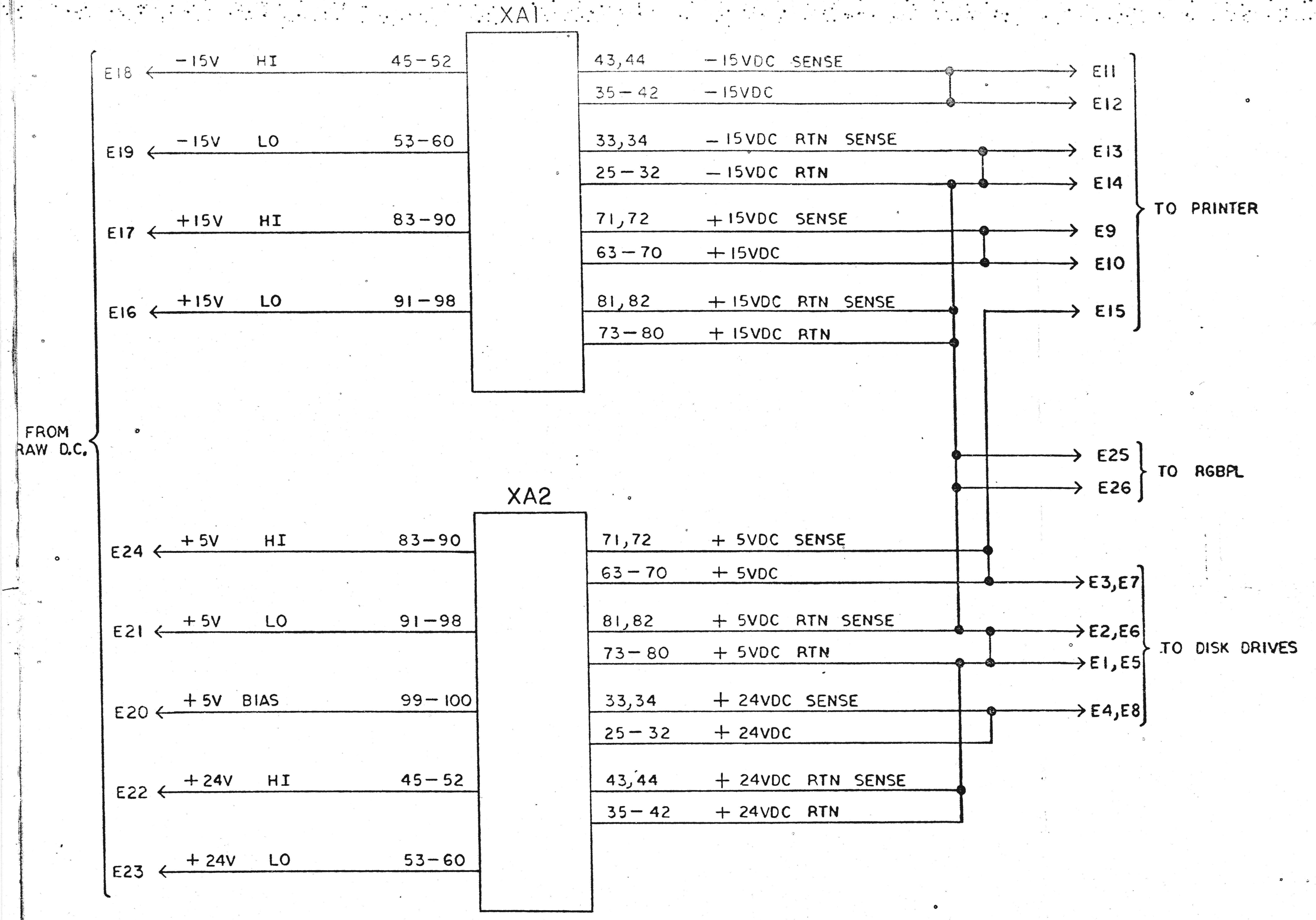
DEVELOPMENT REV D3


XA1
E18 −15V HI 45−52
43,44 −15VDC SENSE E11
35−42 −15VDC E12
E19 −15V LO 53−60
33,34 −15VDC RTN SENSE E13
25−32 −15VDC RTN E14
E17 +15V HI 83−90
71,72 +15VDC SENSE E9
63−70 +15VDC E10
TO PRINTER
E16 +15V LO 91−98
81,82 +15VDC RTN SENSE E15
73−80 +15VDC RTN
FROM RAW D.C.
E25
E26
TO RGBPL
XA2
E24 +5V HI 83−90
71,72 +5VDC SENSE
63−70 +5VDC E3,E7
E21 +5V LO 91−98
81,82 +5VDC RTN SENSE E2,E6
73−80 +5VDC RTN E1,E5
TO DISK DRIVES
E20 +5V BIAS 99−100
33,34 +24VDC SENSE E4,E8
25−32 +24VDC
E22 +24V HI 45−52
43,44 +24VDC RTN SENSE
35−42 +24VDC RTN
E23 +24V LO 53−60

23630

J		K	
G		H	
E		F	
C		D	
A	7546 9-17-76	B	

REVISIONS

NEXT ASSY. 23400

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED TOLERANCES ARE
LINEAR − ANGULAR −
MATERIAL
HEAT TREAT
FINISH

DRAWN	F. MATSUMOTO	DATE 3-12-76
CHECKED	D. Gronberg	9/15/76
ENGR	R Man	9-15-76
MFG	S FRATER	9/16/76

Diablo Systems Incorporated
Hayward California 94545

WIRING DIAGRAM, RGBPN
POWER DISTRIBUTION

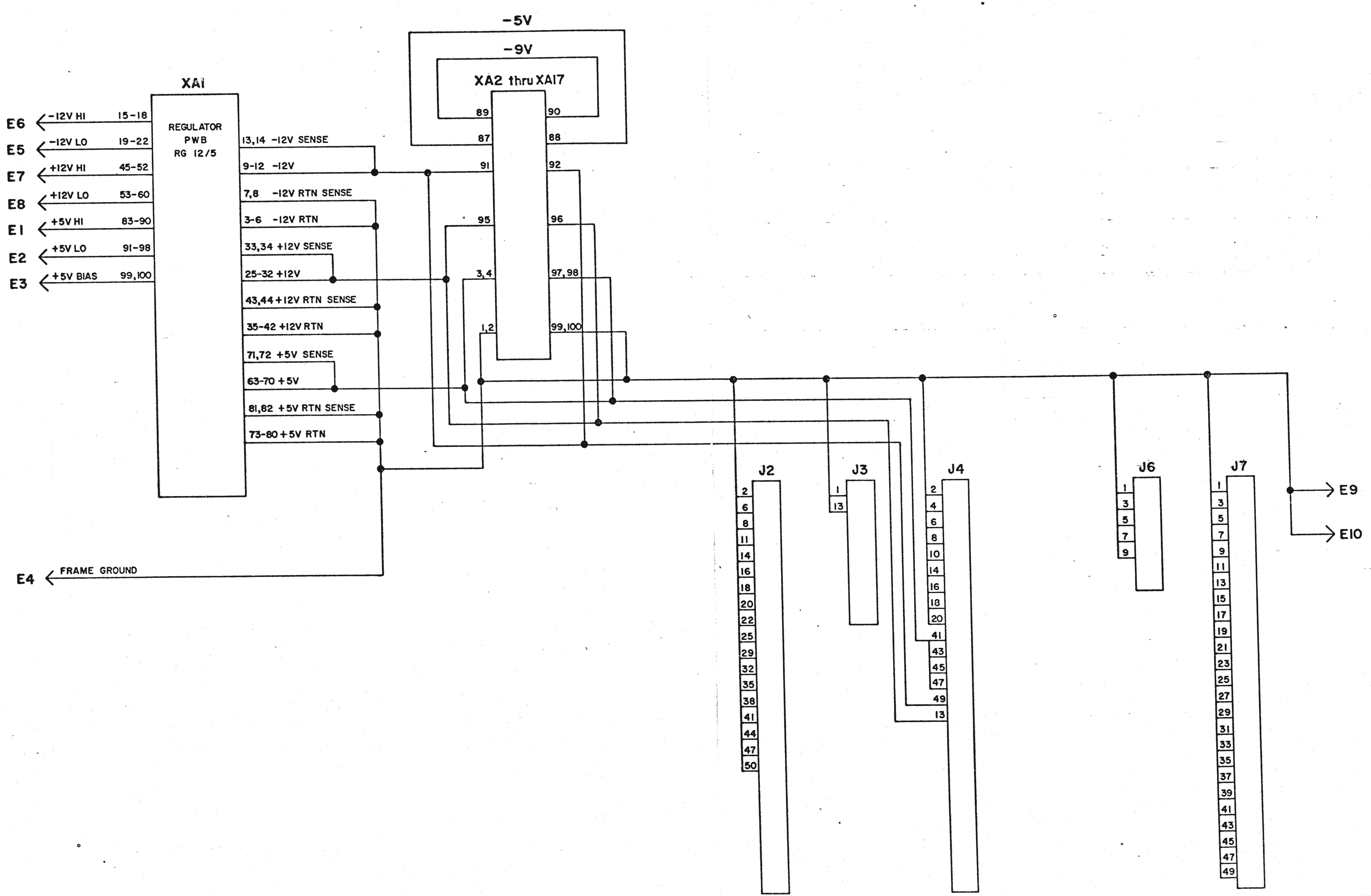
SCALE — SHEET 1 TOT SH 3

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SIZE C 23630

FORM 100-3 DEC 69

DWG NO	DEVELOPMENT REV
23622-XX	D3


XA1
REGULATOR PWB RG 12/5
E6 -12V HI 15-18
E5 -12V LO 19-22
E7 +12V HI 45-52
E8 +12V LO 53-60
E1 +5V HI 83-90
E2 +5V LO 91-98
E3 +5V BIAS 99,100
13,14 -12V SENSE
9-12 -12V
7,8 -12V RTN SENSE
3-6 -12V RTN
33,34 +12V SENSE
25-32 +12V
43,44 +12V RTN SENSE
35-42 +12V RTN
71,72 +5V SENSE
63-70 +5V
81,82 +5V RTN SENSE
73-80 +5V RTN
E4 FRAME GROUND
-5V
-9V
XA2 thru XA17
89
90
87
88
91
92
95
96
3,4
97,98
1,2
99,100
J2
2 6 8 11 14 16 18 20 22 25 29 32 35 38 41 44 47 50
J3
1 13
J4
2 4 6 8 10 14 16 18 20 41 43 45 47 49 13
J6
1 3 5 7 9
J7
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
E9
E10

SCHEMATIC DIAGRAM

DRAWN ED A.	DATE 4-5-76	Diablo Systems Incorporatec Hayward, California 94545
CHECKED D. Gronberg	DATE 9/14/76	THESE DRAWINGS AND OR SPECIFICATIONS, AND THE DATA CONTAINED THERE
ENGR L. Pham	DATE 14 SEP 76	ARE THE EXCLUSIVE PROPERTY OF DIABLO SYSTEMS INC ISSUED IN STR CONFIDENCE AND SHALL NOT, WITHOUT THE PRIOR WRITTEN PERMISSION
MFG S FRATER	DATE 9/14/76	DIABLO SYSTEMS INC. BE SHOWN OR DISCLOSED IN ANY MANNER TO ANY OTH PERSON, OR BE COPIED, REPRODUCED OR USED FOR ANY PURPOSE WHATS EVER, EXCEPT THE MANUFACTURE OF ARTICLES FOR DIABLO SYSTEMS, INC
FIRST USED (NEXT ASSY) 23400		SCHEMATIC: RGBPL POWER DISTRIBUTION
SHEET 1	TOT SHT 14	SIZE D — DWG NO 23622-XX

REV	E.C.O. NO.
A	7543 9-16-76

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Diablo Systems Incorporated
A Xerox Company

TITLE	MODEL	DWG NO.	REV
SIGNAL LIST, RGBPL	3200	23622-XX	A

DRAWN	DATE		SIGNAL LIST SHEET	SHEET	OF
R. MATSUMOTO	8/31/76	* SIGNAL ORIGIN	1 OF 11	4	14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- A ERROR														*58	58				
- A OUT														17	*17				
+ ACTIVE												37	*38						
- AUTO HD UNLD OFF											*55					55			
+ BLINK												50	*50						
- BOARD EN/-SEL 0-16K								48/49											
- BOARD EN/-SEL 16-32K							48/50												
- BOARD EN/-SEL 32-48K						48/51													
- BOARD EN/-SEL 48/64K					48/52														
- BOOT									12										*J4-7
+ BOOT									13										*J4-5
- BOOT EN									*6	6									
+ BUSY A														53	*53				
+ BUSY C															*61	59			
+ B0												40	*40						
+ B1												41	*41						
+ B2												42	*42						
+ B3												43	*43						
+ B4												44	*44						
+ (B5 + Y1)												45	*45						
+ (B6 ⊕ B5)												46	*46						
+ B7														5	*5	5			
+ B7 (CURSOR)												47	*47						
- B7														7	*7	6			
- B7D														19	*19				

Diablo Systems Incorporated
A Xerox Company

TITLE
SIGNAL LIST, RGBPL

MODEL
3200

DWG NO.
23622-XX

REV.
A

DRAWN
R. MATUSMOTO

DATE
8/31/76

* SIGNAL ORIGIN

SIGNAL LIST SHEET
2 OF 11

SHEET
5

OF
14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- CARRIAGE READY		18																	*J2-26
- CARRIAGE STROBE		*27																	J2-17
+ CC0									*16	16	16								
+ CC1									*17	17	17								
- CHECK		22																	*J2-12
+ CHIP EN					53	53	53	53		*53									
+ CK0															24	*24			
+ CK1															25	*25			
- CK1															23	*23			
+ CK2															26	*26			
+ CLOCK 01									*43	43									
+ CLOCK 02	65	65	65	65	65	65	65	65	*65	65	65								
+ CLOCK 03									*61	61	61	61	61						
+ CLOCK 04									*62	62	62	62	62						
+ CLR TO SEND			17																*J3-9
- CLR DIR DOR															*35	35			
- CNT WC														54	*54				
+ COMM CLOCK		44	44						*44										
- CONTROL				13															*J4-46
- COVER OPEN		37																	*J2-5
+ CP BUF DATA 0				*40															J4-33
+ CP BUF DATA 1				*22															J4-34
+ CP BUF DATA 2				*38															J4-35
+ CP BUF DATA 3				*24															J4-36
+ CP BUF DATA 4				*36															J4-37
+ CP BUF DATA 5				*34															J4-38
+ CP BUF DATA 6				*32															J4-39
+ CP BUF DATA 7				*30															J4-40
+ CP DATA 0				25															*J4-21
+ CP DATA 1				14															*J4-22
+ CP DATA 2				23															*J4-23
+ CP DATA 3				12															*J4-24
+ CP DATA 4				21															*J4-25
+ CP DATA 5				10															*J4-26
+ CP DATA 6				19															*J4-27
+ CP DATA 7				16															*J4-28
+ CP DEV ADDR 0				*20															J4-32
+ CP DEV ADDR 1				*15															J4-31
+ CP DEV ADDR 2				*18															J4-30
+ CP DEV ADDR 3				*17															J4-29

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Diablo Systems Incorporated A Xerox Company	TITLE SIGNAL LIST, RGBPL		MODEL 3200	DWG NO 23622-XX		REV A
	DRAWN R. MATSUMOTO	DATE 8/31/76	* SIGNAL ORIGIN	SIGNAL LIST SHEET 3 OF 11	SHEET 6	OF 14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEMØ4 XA6	MEMØ4 XA7	MEMØ4 XA8	MEMØ4 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- CP ENABLE				*28															J4-42
- CP OUT				*35															J4-11
- CP RESET				*29															J4-17
+ CP SYNC				31															J4-15
+ CR Ø														*43	43				
+ CR 1														*44	44				
+ CR 2														*45	45				
+ CR 3														*51	51				
+ CSR OUT ENABLE														*37	37	37			
+ CSR 7															*38	38			
- CYC ON WRITE															*32	32			
- CYC OUT ENABLE														*36	36	36			
- CYC ZERO															69	*69			
+ DATA Ø	79	*79	*79	*79	*79	*79	*79	*79	*79	*79	79	79	79	*79	*79	*79			
+ DATA 1	80	*80	*80	*80	*80	*80	*80	*80	*80	*80	80	80	80	*80	*80	*80			
+ DATA 2	81	*81	*81	*81	*81	*81	*81	*81	*81	*81	81	81	*81	*81	*81	*81			
+ DATA 3	82	*82	*82	*82	*82	*82	*82	*82	*82	*82	82	82	*82	*82	*82	*82			
+ DATA 4	83	*83	*83	*83	*83	*83	*83	*83	*83	*83	83	83	*83	*83	*83	*83			
+ DATA 5	84	*84	*84	*84	*84	*84	*84	*84	*84	*84	84	84	84	*84	*84	*84			
+ DATA 6	85	*85	*85	*85	*85	*85	*85	*85	*85	*85	85	85	85	*85	*85	*85			
+ DATA 7	86	*86	*86	*86	*86	*86	*86	*86	*86	*86	86	86	86	*86	*86	*86			
+ DATA 8					*77	*77	*77	*77	77	*77	77								
- DATA BIT 1		*11																	J2-37
- DATA BIT 2		*12																	J2-36
- DATA BIT 3		*13																	J2-39
- DATA BIT 4		*9																	J2-33
- DATA BIT 5		*10																	J2-40
- DATA BIT 6		*8																	J2-42
- DATA BIT 7		*15																	J2-43
- DATA BIT 8		*17																	J2-45
- DATA BIT 9		*6																	J2-46
- DATA BIT 10		*41																	J2-[illegible]

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Diablo Systems Incorporated
A Xerox Company

TITLE: SIGNAL LIST, RGBPL
MODEL: 3200
DWG NO. 23622-XX
REV. A
DRAWN: R. MATSUMOTO
DATE: 8/31/76
* SIGNAL ORIGIN
SIGNAL LIST SHEET 4 OF 11
SHEET 7
OF 14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEMØ4 XA6	MEMØ4 XA7	MEMØ4 XA8	MEMØ4 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- DATA BIT 11		*33																	J2-9
- DATA BIT 12		*24																	J2-10
+ DATA SET READY			15																*J3-11
+ DATA TERM RDY			*12																J3-14
+ DATA TO MEMORY														*16	16				
+ DEV ADDR Ø	66	66	66	66	66	66	66	66	*66	66	66	66	66	66					
+ DEV ADDR 1	67	67	67	67	67	67	67	67	*67	67	67	67	67	67					
+ DEV ADDR 2	68	68	68	68	68	68	68	68	*68	68	68	68	68	68					
+ DEV ADDR 3	69	69	69	69	69	69	69	69	*69	69	69	69	69	69					
+ DEV ADDR 4	70	70	70	70	70	70	70	70	*70	70	70	70	70	70					
+ DEV ADDR 5	71	71	71	71	71	71	71	71	*71	71	71	71	71	71					
+ DEV ADDR 6	72	72	72	72	72	72	72	72	*72	72	72	72	72	72					
+ DEV ADDR 7	73	73	73	73	73	73	73	73	*73	73	73	73	73	73					
- DEV EN									*63	63									
+ DIM												49	*49						
+ DIR CLK															*73	73			
- DISK A RDY																51			*J2-26
- DISK B RDY																50			*J2-28
- DISK 8 SELECT																*9			J2-42
- DMA CLK										*9	9	9	9	10	10				
- DMA EN									10	*10	10								
+ DMAR														8	*8				
+ DMA RD CLK										*13	13	13	13	13	13				
- DMA REQ										12	12	12	12	*12	12				
- DMA P OUT (-PIN)										*14					14				
- DMA P IN (-TV P)										15	14/15		*14						
+ DMA R/$\overline{W}$									*11	11	11	11	*11	11	*11				
+ DOR CLK															*72	72			
- DOR OUT															*21	21			
+ DOR SØ															*74	74			
+ DOR S1															*75	75			
+ DTA EQL															70	*70			
- DTA ERR														46	46	*46			

Diablo Systems Incorporated
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TITLE	MODEL	DWG NO.	REV.
SIGNAL LIST, RGBPL	3200	23622-XX	A

DRAWN	DATE		SIGNAL LIST SHEET	SHEET	OF
R. MATSUMOTO	8/31/76	* SIGNAL ORIGIN	5 OF 11	8	14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- EN KEY DATA				*26															J4-44
- ERROR STOP															*39	39			
+ F CLK															27	*27			
- FDK P (-P OUT)													15		*15				
+ FFLG														18	*18				
+ FORCE FILL														*41		41			
- FRAME												*56	56						
+ FULL												*53	53						
- GATED DMA RD CLK														40	*41	40			
+ HOR DR												*6							J6-2

Diablo Systems Incorporated
A Xerox Company

TITLE
SIGNAL LIST, RGBPL

MODEL
3200

DWG NO.
23622-XX

REV.
A

DRAWN
R. MATSUMOTO

DATE
8/31/76

* SIGNAL ORIGIN

SIGNAL LIST SHEET
6 OF 11

SHEET
9

OF
14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- IN	75	75	75	75	75	75	75	75	*75	75	75	75	75	75					
- INDEX A																49			*J7-30
- INDEX B																48			*J7-32
- INT ACK 0									*37	37									
- INT ACK 1			49						*49										
- INT ACK 2									*53										
- INT ACK 3				57					*57										
- INT ACK 4									*49			49	49						
- INT ACK 5		55							*55										
- INT ACK 6									*51										
- INT ACK 7									*46					46					
- INT P IN														15					* GND
- INT P OUT														*14					
- INT REQ 0									36	*36									
- INT REQ 1			*48						48										
- INT REQ 2									52										
- INT REQ 3				*56					56										
- INT REQ 4									58			58	58						
- INT REQ 5		*54							54										
- INT REQ 6									50										
- INT REQ 7									38	38				*38					
+ I/O EN									*45	45									
- KY STB				9															*J4-50

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Diablo Systems Incorporated A Xerox Company	TITLE SIGNAL LIST, RGBPL		MODEL 3200	DWG NO 23622-XX	REV A
	DRAWN R. MATSUMOTO	DATE 8/31/76	* SIGNAL ORIGIN	SIGNAL LIST SHEET 7 OF 11	SHEET 10 OF 14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEMØ4 XA6	MEMØ4 XA7	MEMØ4 XA8	MEMØ4 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
+ LC TAIL												51	*51						
- LD CYC															*31	31			
- LD HD A																*13			J7-20
- LD HD B																*12			J7-22
- LOAD DISK FILE CMD														*61		61			
- LO WRITE I																*45			J7-46
- LINE 25												*60	60						
+ MEM ADDR Ø					20	20	20	20	*20	20	20	20	*20	*20					
+ MEM ADDR 1					21	21	21	21	*21	21	21	21	*21	*21					
+ MEM ADDR 2					22	22	22	22	*22	22	22	22	*22	*22					
+ MEM ADDR 3					23	23	23	23	*23	23	23	23	*23	*23					
+ MEM ADDR 4					24	24	24	24	*24	24	24	24	*24	*24					
+ MEM ADDR 5					25	25	25	25	*25	25	25	25	*25	*25					
+ MEM ADDR 6					26	26	26	26	*26	26	26	26	*26	*26					
+ MEM ADDR 7					27	27	27	27	*27	27	27	27	*27	*27					
+ MEM ADDR 8					28	28	28	28	*28	28	28	28	*28	*28					
+ MEM ADDR 9					29	29	29	29	*29	29	29	29	*29	*29					
+ MEM ADDR 10					30	30	30	30	*30	30	30	30	*30	*30					
+ MEM ADDR 11					31	31	31	31	*31	31	31	31	*31	*31					
+ MEM ADDR 12					32	32	32	32	*32	32	32	32	*32	*32					
+ MEM ADDR 13					33	33	33	33	*33	33	33	33	*33	*33					
+ MEM ADDR 14					34	34	34	34	*34	34	34	34	*34	*34					
+ MEM ADDR 15					35	35	35	35	*35	35	35	35	*35	*35					
+ MEM BUS EN					19	19	19	19	*19	*19									
- MEM PARITY LED										*41									J4-1
+ MEM SPEED									*8	8									
- MEM SPEED					39	39	39	39	39	*39									
- MDM RD DATA			21																*J3-5
- MDM RD CLK			16																[illegible]
- MDM XMIT CLK			18																*J3-4

Diablo Systems Incorporated A Xerox Company	TITLE SIGNAL LIST, RGBPL	MODEL 3200	DWG NO 23622-XX	REV. A
DRAWN R. MATSUMOTO	DATE 8/31/76	* SIGNAL ORIGIN	SIGNAL LIST SHEET 8 OF 11	SHEET 11 OF 14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
- OPTION READY		35																	*J2-7
- OPTION STROBE		*25																	J2-19
- OUT	74	74	74	74	74	74	74	74	*74	74	74	74	74	74					
- PAPER FEED READY		14																	*J2-34
- PAPER FEED STROBE		*29																	J2-15
- PAPER OUT		39																	*J2-3
- P OUT (-FDK P)													15		*15				
- PIN (-DMA P OUT)									*14						14				
- PRINTER READY		16																	*J2-28
- PRINTER SELECT		*20																	J2-24
- PW READY		19																	*J2-27
- PW STROBE		*23																	J2-21
+ READ SYNC															28	*28			
- RD E															*22	22			
- READ C STAT														*62	62	62			
- READ D STAT														*63		63			
- READ E														*64	64				
- READ CLOCK																53			*J7-12
- READ DATA																54			*J7-10
- READ ON B															*33	33			
+ READY									42	*42									
+ RECD SIGNAL DET			13																*J3-15
- REQ INH												*57	57						
+ REQ TO SEND			*19																J3-7
- RESET	78	78	78	*78	78	78	78	78	78	78	78	78	78	78					
- RESTORE PRINTER		*31																	J2-13
- RFH EN					5	5	5	5	5	*5									
- RIBBON LIFT		*21																	J2-23
- RIBBON OUT		26																	*J2-4

Diablo Systems Incorporated
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TITLE	MODEL	DWG NO.	REV.
SIGNAL LIST, RGBPL	3200	23622-XX	A

DRAWN	DATE		SIGNAL LIST SHEET	SHEET	OF
R. MATSUMOTO	8/31/76	* SIGNAL ORIGIN	9 OF 11	12	14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
+ RING IND			29																*J3-18
- RST CLR A1														*77	77	77			
+ RUN									7	*7									J4-3
+ R/$\overline{W}$					18	18	18	18	18	*18									
+ RV VID												48	*48						
- SEEK DIRECTION IN																*7			J7-48
+ SEL RDY															76	*76			
- SELECT 1																*15			J7-8
- SELECT 2																*16			J7-6
- SELECT 3																*17			J7-4
- SELECT 4																*18			J7-2
- SEL 0-16K/-BOARD EN								49/48											
- SEL 16-32K/-BOARD EN							50/48												
- SEL 32-48K/-BOARD EN						51/48													
- SEL 48-64K/-BOARD EN					52/48														
+ SELECTED INDEX														57	57	*57			
+ SENSE LOWER CASE				11															*J4-48
- SHIFT												52	*52						
+ SIGNAL QUALITY			14																*J3-16
+ SPECIAL FUNCTION 12			*9																J3-23
+ SPECIAL FUNCTION 14			*20																J3-2
+ SPECIAL FUNCTION 23			*27																J3-20
+ SPECIAL FUNCTION 25			*11																J3-21/24
- STEP																*11			J7-24
+ STEP CMD														*42		42			
+ ST0A														47	*47				
+ ST1A														48	*48				
+ ST2A														49	*49				
+ ST3A														50	*50				
- STOP									*41										
- SYSTEM RESET				37					[illegible]										[illegible]
+ SYNC	76	76	76	76	76	76	76	76	*76	76	76	76	76	76					
- SUDO CLK															78	*78			

Diablo Systems Incorporated
A Xerox Company

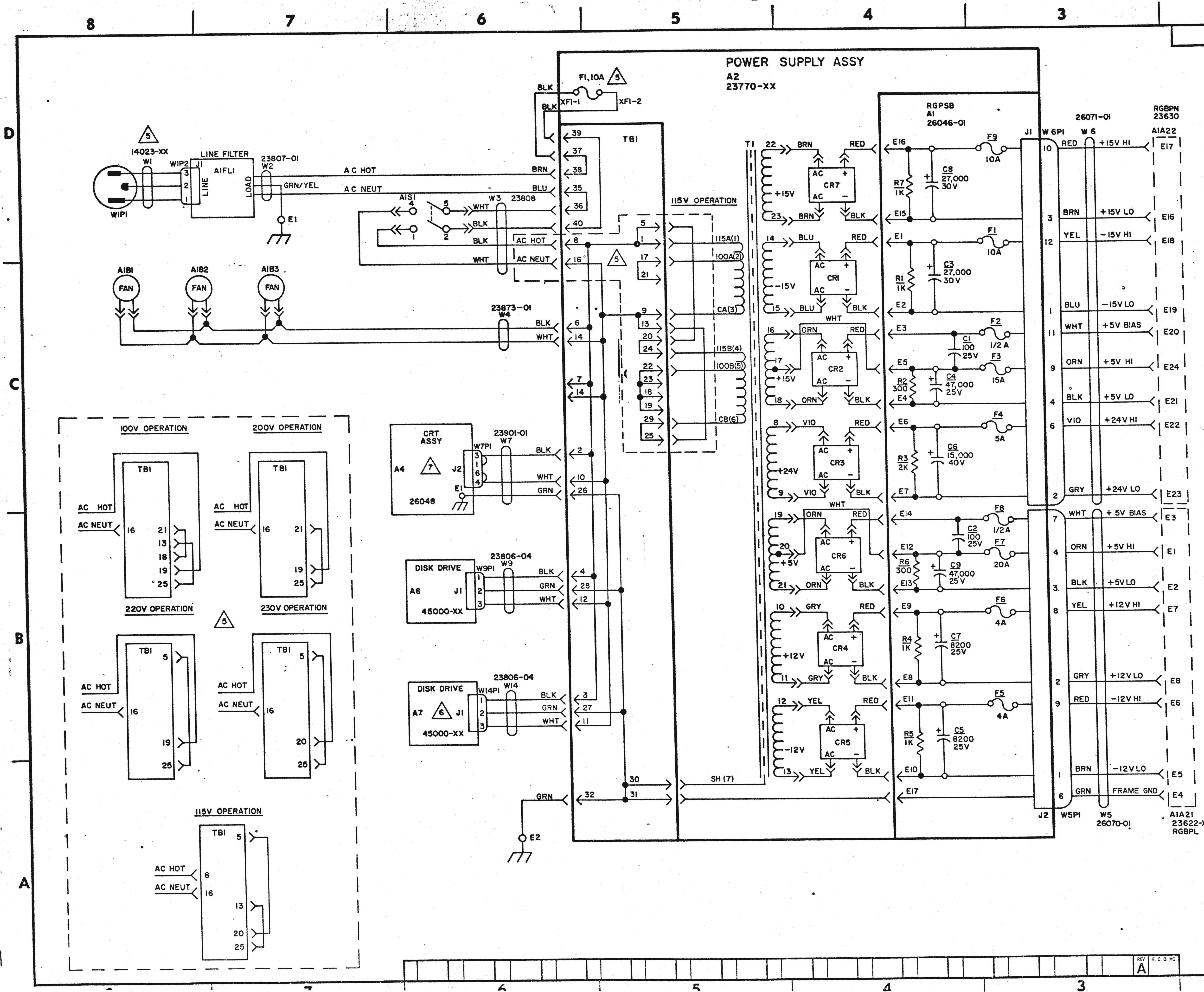
TITLE	MODEL	DWG NO.	REV.
SIGNAL LIST, RGBPL	3200	23622-XX	A

DRAWN	DATE		SIGNAL LIST SHEET	SHEET	OF
R. MATSUMOTO	8/31/76	* SIGNAL ORIGIN	10 OF 11	13	14

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
+ T CLK															20	*20			
- THIS UNIT COMMAND														*65		65			
- TMR														60	*60				
- TO IDLE														52	*52				
- TRACK 00																47			*J7-38
- TV P (-DMA P IN)										15	14/15		*14						
- VERT DR												*7							J6-8
+ VIDEO												*5							J6-10
+ W CLK TIME															67	*67			
- W CLK TIME															68	*68			
- WCZ														*55	55				
- WRITE DATA AND CLK																*8			J7-44
- WRITE DATA PHASE															71	71			
- WFLG														6	*6				
- WRITE GATE																*14			J7-18
+ WRITE ON B															*34	34			
- WRITE PROTECT																52			*J7-16

Diablo Systems Incorporated A Xerox Company	TITLE SIGNAL LIST, RGBPL	MODEL 3200	DWG NO. 23622-XX	REV A
	DRAWN R. MATSUMOTO	DATE 8/31/76	* SIGNAL ORIGIN	
	SIGNAL LIST SHEET 11 OF 11	SHEET 14	OF 14	

SIGNAL NAME	SPARE XA2	RGPNT XA3	RGCOM XA4	RGKEY XA5	MEM04 XA6	MEM04 XA7	MEM04 XA8	MEM04 XA9	PROC2 XA10	RGDMA XA11	SPARE XA12	TVSWP XA13	TVDMA XA14	RGFCA XA15	RGFCB XA16	RGFCC XA17			I/O
+ XEQU														*56	56				
- XMIT DATA			*23																J3-3
- XMIT TIMING EXT			*25																J3-22
SPARE 1												8							J6-4
SPARE 2												10							J6-6
SPARE 3														59	59				
SPARE 4																10			J7-40
SPARE 5												63	63						


8
7
6
5
4
3
D
C
B
A
POWER SUPPLY ASSY
A2
23770-XX
F1,10A
5
XF1-1
XF1-2
BLK
BLK
5
14023-XX
W1
W1P2
J1
LINE FILTER
23807-01
W2
A1FL1
LINE
LOAD
W1P1
GRN/YEL
AC HOT
AC NEUT
BRN
BLU
E1
A1S1
4
5
1
2
W3
23808
WHT
BLK
BLK
WHT
AC HOT
AC NEUT
A1B1
A1B2
A1B3
FAN
FAN
FAN
23873-01
W4
BLK
WHT
TB1
39
37
38
35
36
40
8
16
6
14
7
14
2
10
26
4
28
12
3
27
11
32
30
31
115V OPERATION
5
1
17
21
9
13
20
24
22
23
18
19
29
25
115A(1)
100A(2)
CA(3)
115B(4)
100B(5)
CB(6)
SH (7)
T1
CRT ASSY
A4
7
J2
W7P1
23901-01
W7
26048
E1
BLK
WHT
GRN
DISK DRIVE
A6
J1
W9P1
23806-04
W9
45000-XX
BLK
GRN
WHT
DISK DRIVE
A7
6
J1
W14P1
23806-04
W14
45000-XX
BLK
GRN
WHT
GRN
E2
100V OPERATION
200V OPERATION
TB1
AC HOT
AC NEUT
16
21
13
18
19
25
TB1
AC HOT
AC NEUT
16
21
19
25
220V OPERATION
230V OPERATION
5
TB1
AC HOT
AC NEUT
16
5
19
25
TB1
AC HOT
AC NEUT
16
5
20
25
115V OPERATION
TB1
5
AC HOT
8
AC NEUT
16
13
20
25
22
BRN
RED
AC
+
CR7
AC
−
+15V
23
BRN
BLK
14
BLU
RED
AC
+
CR1
AC
−
−15V
15
BLU
BLK
WHT
16
ORN
RED
17
AC
+
CR2
AC
−
+15V
18
ORN
BLK
8
VIO
RED
AC
+
CR3
AC
−
+24V
9
VIO
BLK
WHT
19
ORN
RED
20
AC
+
CR6
AC
−
+5V
21
ORN
BLK
10
GRY
RED
AC
+
CR4
AC
−
+12V
11
GRY
BLK
12
YEL
RED
AC
+
CR5
AC
−
−12V
13
YEL
BLK
RGPSB
A1
26046-01
E16
E15
R7
1K
C8
27,000
30V
F9
10A
E1
E2
R1
1K
C3
27,000
30V
F1
10A
E3
C1
100
25V
F2
1/2 A
E5
R2
300
E4
C4
47,000
25V
F3
15A
E6
R3
2K
E7
C6
15,000
40V
F4
5A
E14
C2
100
25V
F8
1/2A
E12
R6
300
E13
C9
47,000
25 V
F7
20A
E9
R4
1K
E8
C7
8200
25V
F6
4A
E11
R5
1K
E10
C5
8200
25V
F5
4A
E17
J1
W6P1
W6
26071-01
RGBPN
23630
A1A22
10
RED
+15V HI
E17
3
BRN
+15V LO
E16
12
YEL
−15V HI
E18
1
BLU
−15V LO
E19
11
WHT
+5V BIAS
E20
9
ORN
+5V HI
E24
4
BLK
+5V LO
E21
6
VIO
+24V HI
E22
2
GRY
+24V LO
E23
7
WHT
+ 5V BIAS
E3
4
ORN
+5V HI
E1
3
BLK
+5V LO
E2
8
YEL
+12V HI
E7
2
GRY
+12V LO
E8
9
RED
−12V HI
E6
1
BRN
−12V LO
E5
6
GRN
FRAME GND
E4
J2
W5P1
W5
26070-01
A1A21
23622-XX
RGBPL

23676-01
ON DWG

DEVELOPMENT REV
D2

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE IS SPECIFIED IN MICROFARADS.
2. RESISTANCE IS IN OHMS.
3. RESISTORS ARE 1 WATT.
4. ALL FUSES ARE SLOW BLOW TYPE.

△5 FOR 200V − 230V OPERATION, POWER CORD W1 IS NOT SUPPLIED AND FUSE F1 IS CHANGED TO 6.25A. FOR OPERATION AT OTHER THAN 115 V, MAKE CHANGES TO TB1 AS SHOWN. NO CHANGES ARE REQUIRED IN PRIMARY LEADS OF TRANSFORMER (T1), OR IN LEADS OF 115V AUXILIARY DEVICES, OR FOR OPERATION FROM 47 TO 63HZ.

△6 OPTIONAL DISK DRIVE.

△7 INSTALLED ON 23932-XX ASSY ONLY.

ADVANCE RELEASE

SCHEMATIC DIAGRAM

DRAWN ED ADAMS
DATE 10-28-76
CHECKED
DATE
ENGR
DATE
MFG
DATE

Diablo Systems Incorporate
Hayward, California 94545

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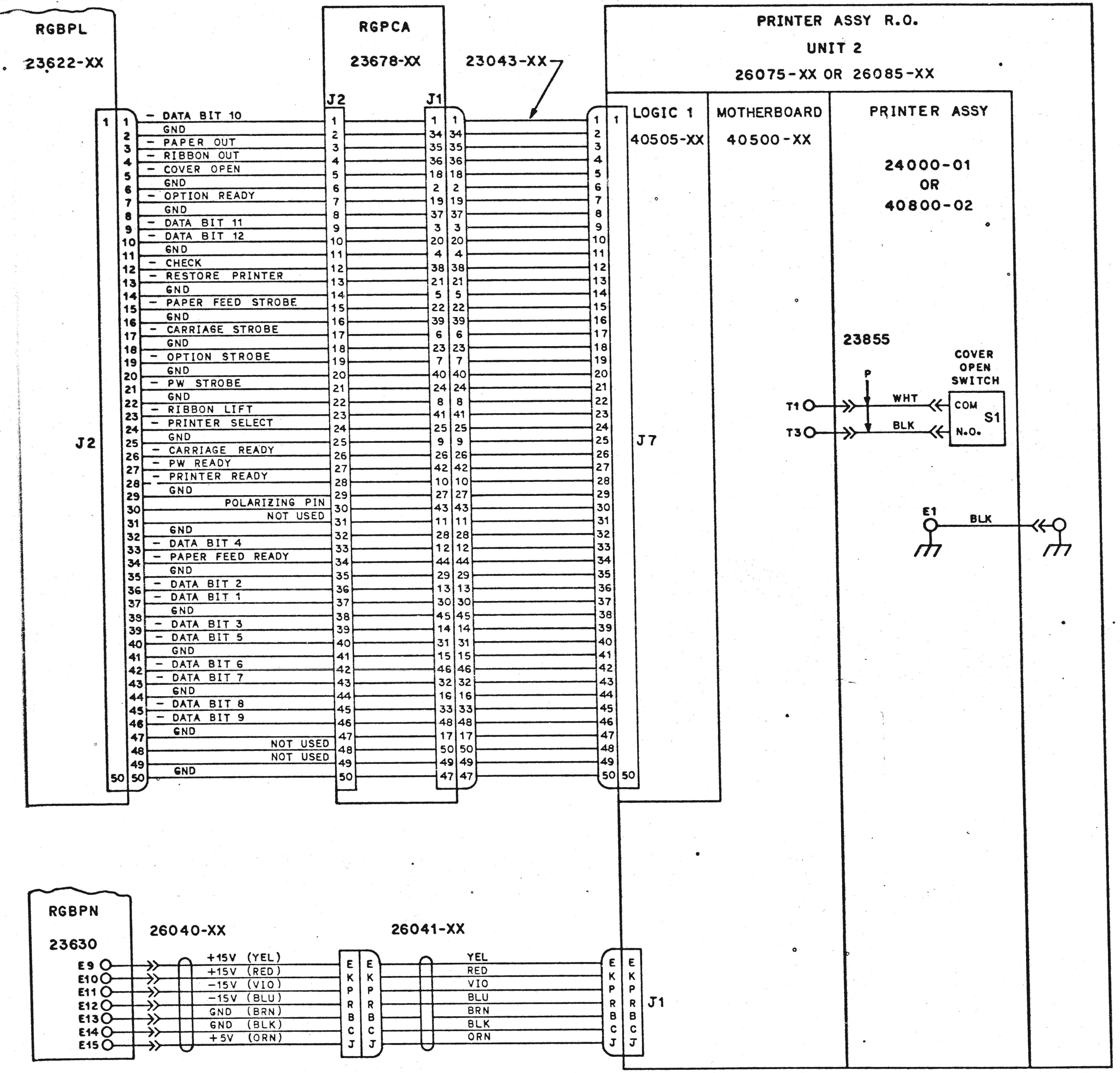
FIRST USED (NEXT ASSY) 23400-XX & 23932-XX
SCHEMATIC, POWER DISTRIBUTION
SHEET 1
TOT SHT 1
SIZE D
DWG NO 23676-01
REV A
E.C.O. NO.

2
1

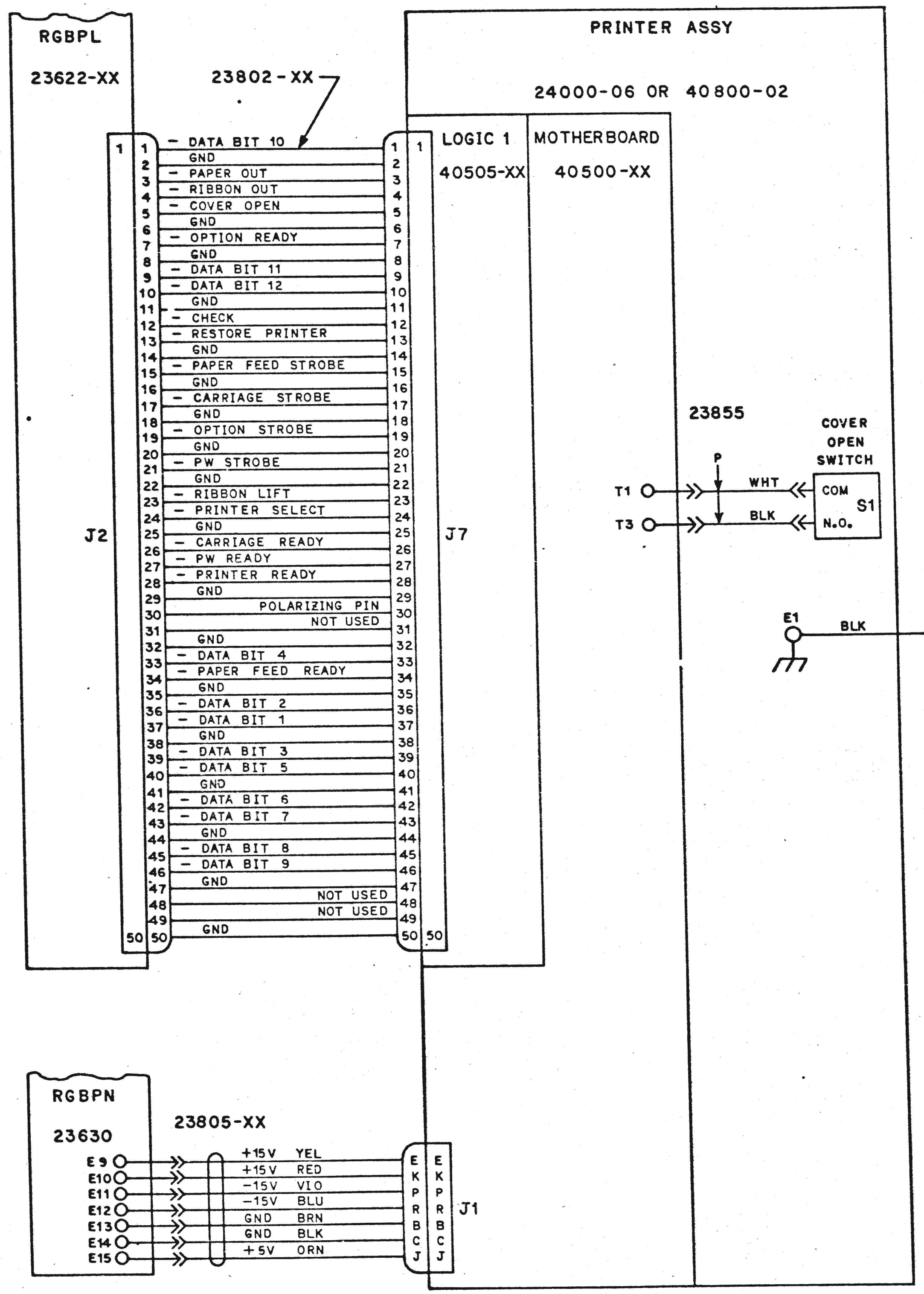
49


RGBPL
23622-XX
J2
RGBPN
23630
E9
E10
E11
E12
E13
E14
E15
26040-XX
+15V (YEL)
+15V (RED)
−15V (VIO)
−15V (BLU)
GND (BRN)
GND (BLK)
+5V (ORN)
RGPCA
23678-XX
J2
J1
23043-XX
26041-XX
YEL
RED
VIO
BLU
BRN
BLK
ORN
E K P R B C J
J1
DATA BIT 10
GND
PAPER OUT
RIBBON OUT
COVER OPEN
OPTION READY
DATA BIT 11
DATA BIT 12
CHECK
RESTORE PRINTER
PAPER FEED STROBE
CARRIAGE STROBE
OPTION STROBE
PW STROBE
RIBBON LIFT
PRINTER SELECT
CARRIAGE READY
PW READY
PRINTER READY
POLARIZING PIN
NOT USED
DATA BIT 4
PAPER FEED READY
DATA BIT 2
DATA BIT 1
DATA BIT 3
DATA BIT 5
DATA BIT 6
DATA BIT 7
DATA BIT 8
DATA BIT 9
NOT USED
NOT USED
PRINTER ASSY R.O.
UNIT 2
26075-XX OR 26085-XX
LOGIC 1
40505-XX
MOTHERBOARD
40500-XX
PRINTER ASSY
24000-01
OR
40800-02
J7
23855
T1
T3
P
WHT
BLK
COVER OPEN SWITCH
COM
N.O.
S1
E1
BLK

ADVANCE RELEASE

23679-01

ON PROCESSOR ASSY WITH CRT (23932-XX), THIS R.O. PRINTER ASSY ( ) AND ASSOCIATED CABLES ARE AN OPTION.


RGBPL
23622-XX
J2
23802-XX
RGBPN
23630
E9
E10
E11
E12
E13
E14
E15
23805-XX
+15V YEL
+15V RED
−15V VIO
−15V BLU
GND BRN
GND BLK
+5V ORN
E K P R B C J
J1
DATA BIT 10
GND
PAPER OUT
RIBBON OUT
COVER OPEN
OPTION READY
DATA BIT 11
DATA BIT 12
CHECK
RESTORE PRINTER
PAPER FEED STROBE
CARRIAGE STROBE
OPTION STROBE
PW STROBE
RIBBON LIFT
PRINTER SELECT
CARRIAGE READY
PW READY
PRINTER READY
POLARIZING PIN
NOT USED
DATA BIT 4
PAPER FEED READY
DATA BIT 2
DATA BIT 1
DATA BIT 3
DATA BIT 5
DATA BIT 6
DATA BIT 7
DATA BIT 8
DATA BIT 9
NOT USED
NOT USED
PRINTER ASSY
24000-06 OR 40800-02
LOGIC 1
40505-XX
MOTHERBOARD
40500-XX
J7
23855
T1
T3
P
WHT
BLK
COVER OPEN SWITCH
COM
N.O.
S1
E1
BLK

23679-02

ON PROCESSOR ASSY WITH PRINTER (23400-XX), THE CRT ASSY ( ) AND ASSOCIATED CABLES ARE REPLACED BY THIS PRINTER ASSY ( ) AND ASSOCIATED CABLES.

Diablo Systems Incorporate

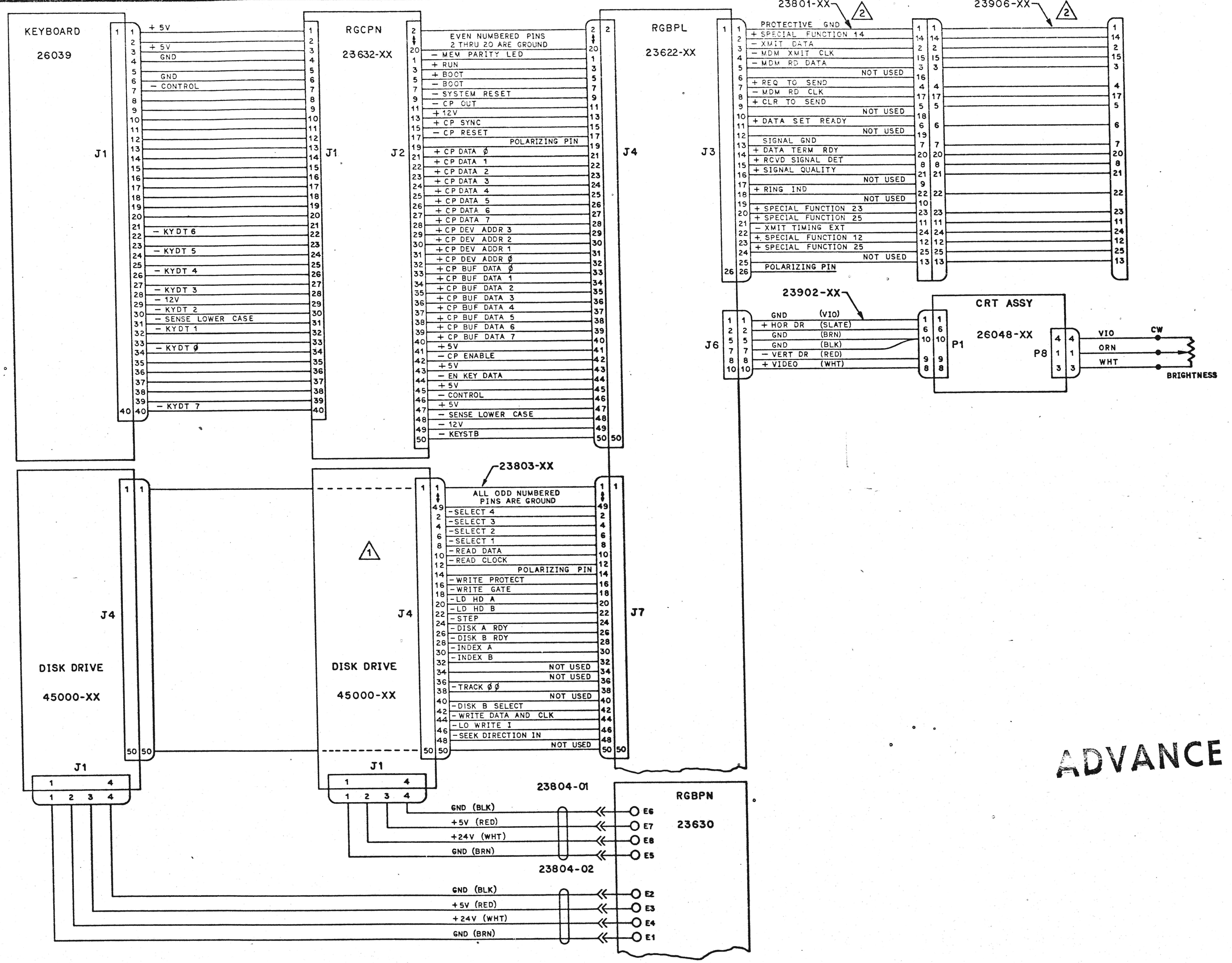
INTERCONNECTION DIAGRAM
SIGNAL AND DC POWER CABLE

12-28-76

1 2

2

23679-XX


KEYBOARD
26039
J1
+5V
+5V
GND
GND
− CONTROL
− KYDT 6
− KYDT 5
− KYDT 4
− KYDT 3
− 12V
− KYDT 2
− SENSE LOWER CASE
− KYDT 1
− KYDT 0
− KYDT 7
RGCPN
23632-XX
J1
J2
EVEN NUMBERED PINS
2 THRU 20 ARE GROUND
− MEM PARITY LED
+ RUN
+ BOOT
− BOOT
− SYSTEM RESET
− CP OUT
+12V
+ CP SYNC
− CP RESET
POLARIZING PIN
+ CP DATA 0
+ CP DATA 1
+ CP DATA 2
+ CP DATA 3
+ CP DATA 4
+ CP DATA 5
+ CP DATA 6
+ CP DATA 7
+ CP DEV ADDR 3
+ CP DEV ADDR 2
+ CP DEV ADDR 1
+ CP DEV ADDR 0
+ CP BUF DATA 0
+ CP BUF DATA 1
+ CP BUF DATA 2
+ CP BUF DATA 3
+ CP BUF DATA 4
+ CP BUF DATA 5
+ CP BUF DATA 6
+ CP BUF DATA 7
+5V
− CP ENABLE
+5V
− EN KEY DATA
+5V
− CONTROL
+5V
− SENSE LOWER CASE
− 12V
− KEYSTB
RGBPL
23622-XX
J4
J3
23801-XX
2
PROTECTIVE GND
+ SPECIAL FUNCTION 14
− XMIT DATA
− MDM XMIT CLK
− MDM RD DATA
NOT USED
+ REQ TO SEND
− MDM RD CLK
+ CLR TO SEND
NOT USED
+ DATA SET READY
NOT USED
SIGNAL GND
+ DATA TERM RDY
+ RCVD SIGNAL DET
+ SIGNAL QUALITY
NOT USED
+ RING IND
NOT USED
+ SPECIAL FUNCTION 23
+ SPECIAL FUNCTION 25
− XMIT TIMING EXT
+ SPECIAL FUNCTION 12
+ SPECIAL FUNCTION 25
NOT USED
POLARIZING PIN
23906-XX
2
23902-XX
J6
GND (VIO)
+ HOR DR (SLATE)
GND (BRN)
GND (BLK)
− VERT DR (RED)
+ VIDEO (WHT)
CRT ASSY
26048-XX
P1
P8
VIO
ORN
WHT
CW
BRIGHTNESS
DISK DRIVE
45000-XX
J4
J1
DISK DRIVE
45000-XX
1
J4
J1
23803-XX
ALL ODD NUMBERED
PINS ARE GROUND
− SELECT 4
− SELECT 3
− SELECT 2
− SELECT 1
− READ DATA
− READ CLOCK
POLARIZING PIN
− WRITE PROTECT
− WRITE GATE
− LD HD A
− LD HD B
− STEP
− DISK A RDY
− DISK B RDY
− INDEX A
− INDEX B
NOT USED
NOT USED
− TRACK 00
NOT USED
− DISK B SELECT
− WRITE DATA AND CLK
− LO WRITE I
− SEEK DIRECTION IN
NOT USED
J7
23804-01
GND (BLK)
+5V (RED)
+24V (WHT)
GND (BRN)
23804-02
GND (BLK)
+5V (RED)
+24V (WHT)
GND (BRN)
RGBPN
23630
E6
E7
E8
E5
E2
E3
E4
E1

NOTES:

1. OPTIONAL DISK DRIVE.
2. CABLES 23801-XX AND 23906-XX ARE PART OF THE EIA OPTION (26084-XX).

ADVANCE RELEASE

Diablo Systems Incorporated

INTERCONNECTION DIAGRAM
SIGNAL AND DC POWER CABLES

MODEL

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO

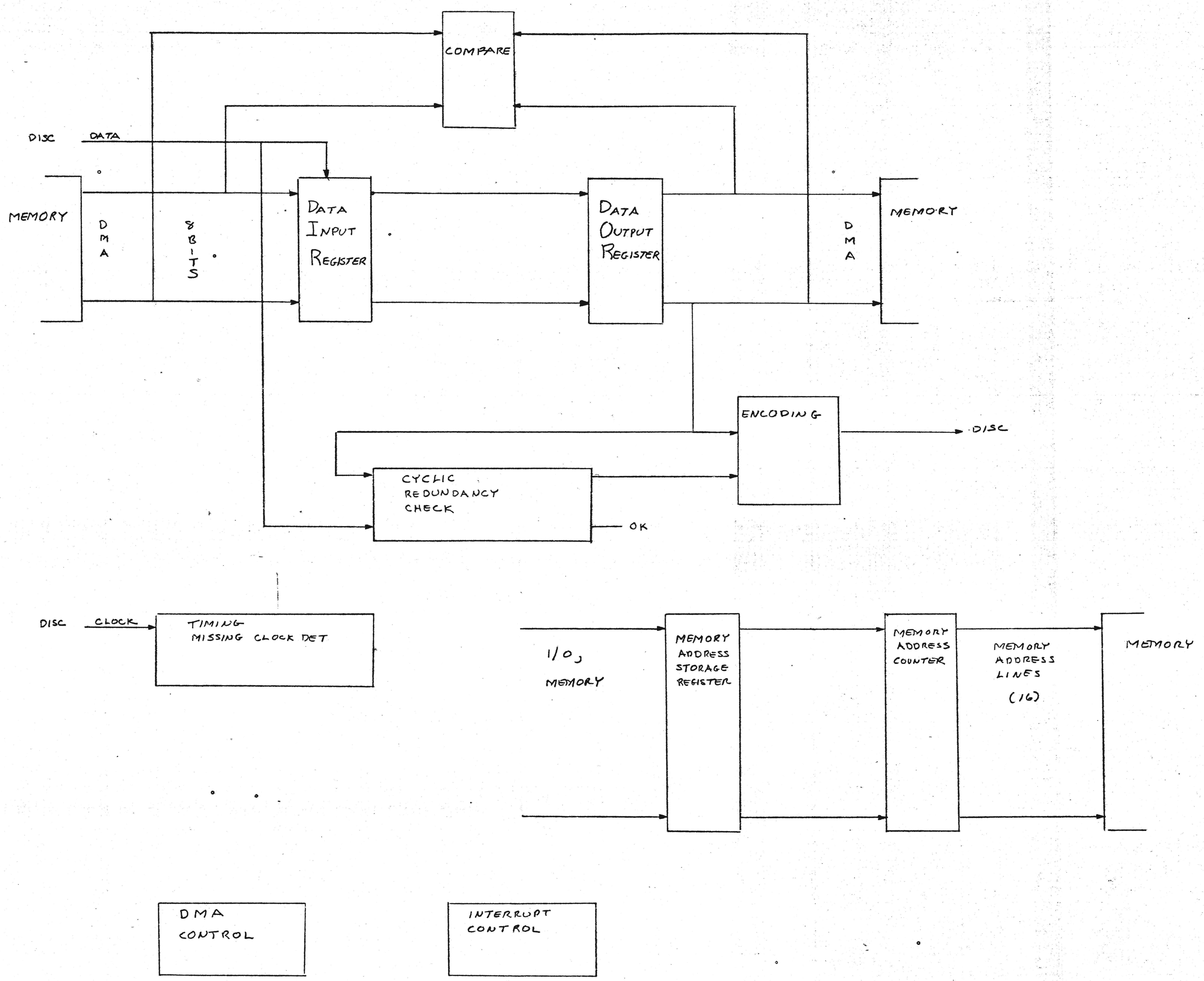
SCHEMATIC INCLUDES SHEETS 1 THRU 2

SHEET 1 TOTAL SHEETS SIZE D

PRODUCT NO 23679 XX

REV

N/C 12-22-76

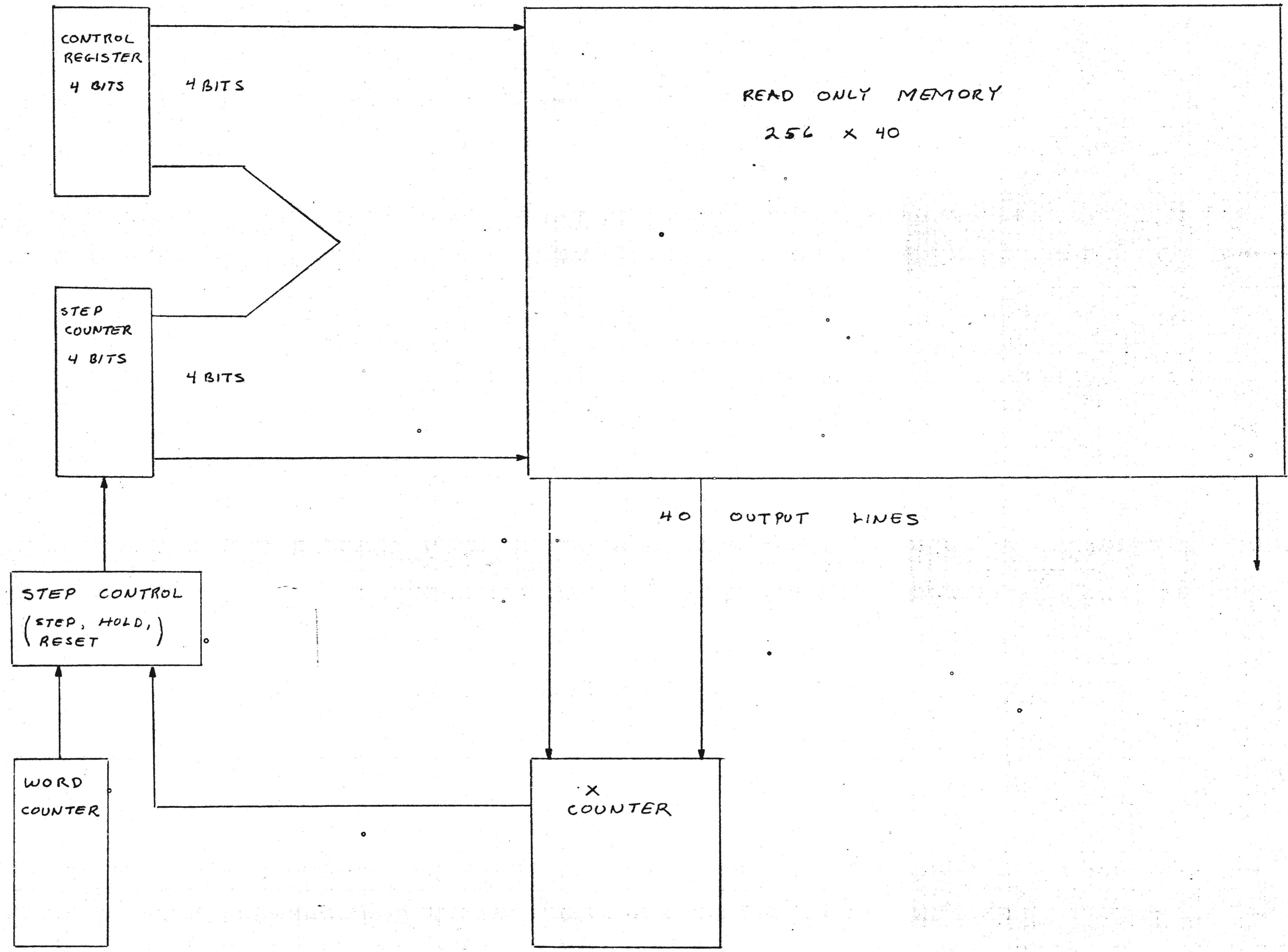

COMPARE
DISC
DATA
MEMORY
DMA
8 BITS
DATA INPUT REGISTER
DATA OUTPUT REGISTER
DMA
MEMORY
ENCODING
DISC
CYCLIC REDUNDANCY CHECK
OK
DISC
CLOCK
TIMING
MISSING CLOCK DET
I/O,
MEMORY
MEMORY ADDRESS STORAGE REGISTER
MEMORY ADDRESS COUNTER
MEMORY ADDRESS LINES
(16)
MEMORY
DMA CONTROL
INTERRUPT CONTROL

BLOCK DIAGRAM
RANGER FLOPPY
DISC CONTROLLER

R SWENSON NOV 16, 19

SHEET 1 OF 2

MAIN CONTROL SEQUENCING


CONTROL REGISTER
4 BITS
4 BITS
STEP COUNTER
4 BITS
4 BITS
READ ONLY MEMORY
256 × 40
40 OUTPUT LINES
STEP CONTROL
(STEP, HOLD, RESET)
WORD COUNTER
X COUNTER

BLOCK DIAGRAM
RANGER FLOPPY
DISC CONTROLLER

R SWENSON NOV 1979

SHEET 2 OF 2

RS

READ SECTOR

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
R	0	00		00		X	4						X				X						X							X																		X	SET UP
R	1	ID AM	DMA →	00			4	X			X	X																										X			X											SEARCH FOR MISSING CLOCK PATTERN
R	2	TRK	D →	ID AM		X	4	X			X	X													X	X										X													COMPARE DISC HEADER AGAINST
		0	D →	TRK		X	3	X			X	X													X	X										X													IMAGE IN MEMORY
		SEC	D →	0		X	2	X			X	X													X	X										X													
		0	D →	SEC		X	1	X			X	X													X	X										X													
		CRC	D →	0		X	0	X			X	X													X	X										X													STEP WHEN X CTR = 0
R	3	CRC	D	CRC				X				X																											X							X			CHECK HEADER CRC; GET DATA MA LO FROM MEMORY
R	4	00		00		X	13						X				X				X		X					X	X		X																X		X=13; GET DATA MA HI; SET UP CRC FOR DATA
R	5	00		00		X	13																	X	X																							WAIT 13 BYTE TIMES
		00		00		X	12																	X	X																							
							↓																	X	X																							
		00		00		X	1																	X	X																							
		00		00		X	0																	X	X																							
R	6	DAM	D →	00		W	N-1	X			X	X									X																	X			X								WAIT FOR & TEST DAM CLOCKS
R	7	D1	D →	DAM		W	N-2	X			X	X									X																			X	X							X	TEST DAM VS MEMORY – DATA READ BEGINS; DATA ADD → MA
R	8	D2	D →	D1		W	N-3	X			X	X								X	X	X																		X								READ DATA; CHECK FOR MISSING CLOCKS
		D3	D →	D2		W	N-4	X			X	X								X	X	X																		X								
		↓	↓	↓			↓	↓			↓	↓								↓	↓	↓																		X								
		1	D →	D		W	1	X			X	X								X	X	X																		X								
		0	D →	1		W	0	X			X	X								X	X	X																		X								
R	9	CRC		0				X												X																				X								LAST DATA BYTE TO MEM; 1ST CRC READ
R	10	CRC						X												X																				X	X						CHECK DATA CRC
R	11																																														WAIT 1 BYTE
R	12																																			X												END OPERATION – GO NOT BUSY; INTERRUPT
																																			|X|											
																																			|X|											
																																			|X|											
																																			|X|											
																																			|X|											
																																			|X|											
																																			|X|											
																																			|↓ ALL OTHER POSITIONS|											

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WS

WRITE SECTOR

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
W	0	00		00		X	4						X				X						X						X																	X	SET UP FOR HEADER SEARCH
W	1	ID AM	D →	00				X			X	X																						X			X										SEARCH FOR MISSING CLOCK PATTERN
W	2	TR_c	D →	ID AM		X	4	X			X	X												X	X										X												HEADER SEARCH: COMPARE DISK HEADER
		0	D →	TR_c		X	3	X			X	X												X	X										X												AGAINST HEADER IMAGE IN MEMORY -
		SE_c	D →	0		X	2	X			X	X												X	X										X												IF DIFFERENT START OVER AT W0
		0	D →	SE_c		X	1	X			X	X												X	X										X												
		CR_c	D →	0		X	0	X			X	X												X	X										X												
W	3	CR_c	D	CR_c				X				X																										X						X			CHECK HEADER CRC; GET DATA MA LO FROM MEM
W	4	00		00		X	16						X				X						X				X																		X		GET DATA MA HI FROM MEMORY; SET X = 16
W	5	00		00			16						X											X	X				X	X																	WAIT 10 BYTE TIMES UNTIL XCTR = 6
		00		00			15						X											X	X				X	X																	
		00		00			↓						X											X	X				X	X																	
		00		00			7						X											X	X				X	X																	
		00		00			6						X											X	X				X	X																	
W	6	00		00	00		5		X				X											X	X					X																	WRITE 4 BYTES OF ZERO
		00		00	00		4		X				X											X	X					X																	
		00		00	00		3		X				X											X	X					X																	
		00		00	00		2		X				X											X	X					X																	
W	7	00	D →	00	00				X		X	X																																			WRITE 1 BYTE OF ZERO, CALL FOR DAM (OR DDAM)
W	8	DAM	D →	00	00				X		X	X									X																									X	1 BYTE OF ZERO (6 TOTAL) NEW MA (DATA FIELD) DAM FROM MEM
W	9	N	D →	DAM	DAM	W	N-1		X		X	X		X		X		X			X	X																									WRITE DATA FIELD START WITH DAM (OR DDAM)
		N-1	D →	N	N	W	N-2		X		X	X		X		X		X			X	X																									WITH MISSING CLOCKS START CRC ACCUMULATION
		↓	D →	↓	↓	W	↓		X		X	X		X		X		X			X	X																									
		0	D →	1	1	W	1		X		X	X		X		X		X			X	X																									
		0-1	D →	0	0	W	0		X		X	X		X		X		X			X	X																									
W	10			0-1	CRC	X	1		X									X	X					X	X																						WRITE CRC
				FF_x	CRC	X	0		X									X	X					X	X																						
W	11			FF_x	FF				X														X					X		X														X				X=10 INTERRUPT OCCURS HERE
W	12			FF_x	FF_x	X	10		X															X	X				X	X														X				WRITE FILL - ALLOW FOR ERASE TIMING
				FF_x	FF_x		9		X															X	X				X	X														X				
				FF_x	FF_x		8		X															X	X				X	X														X				
				FF_x	FF_x		7		X															X	X				X	X														X				
				FF_x	FF_x		6		X															X	X				X	X														X				
W	13						5																	X	X																			X				WAIT FOR TUNNEL ERASE OFF
							4																	X	X																			X				WRITE OFF
							3																	X	X																			X				
							2																	X	X																			X				
							1																	X	X																			X				
							0																	X	X																			X				
W	14																																			X							X				END OPERATION; BUSY RESET
																																				X											
																																				X	ALL OTHER POSITIONS										
																																				X											
																																				↓											

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READ NEXT HEADER

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
H	0	00		00									X				X						X							X																X	SET UP XCTR = 2
H	1	ID AM	D →	00				X			X	X																						X			X										CHECK FOR MISSING CLOCKS
H	2	TR K	D →	ID AM				X			X	X																							X												COMPARE IDAM AGAINST MEMORY
H	3	0	D →	TR K		x	2	X			X	X								X				X	X															X							HEADER DATA TO MEMORY
		SE C	D →	0			1	X			X	X								X				X	X															X							
		0	D →	SE C			0	X			X	X								X				X	X															X							
H	4	CR C		0				X												X																				X							LAST BYTE TO MEMORY
H	5	CR C						X																														X		X	X						DO CRC
H	6																																			X											END OPERATION; BUSY RESET; INTERRUPT
																																				X											
																																				X											
																																				X											
																																				X ALL OTHER POSITIONS											
																																				↓											

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• FORMAT TRACK

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
F	0	00		00									X				X						X							X	X															X	SET UP
F	1	00		00	FF_x	W	N		X	X			X								X	X																									WRITE WC BYTES OF FILL CHARACTERS
		00		00	FF_x		N-1		X	X			X								X	X																									
		00		00	FF_x		↓		X	X			X								X	X																									
		00		00	FF_x		1		X	X			X								X	X																									
		00		00	FF_x		0		X	X			X								X	X																									
F	2	00		00	00	X	3		X				X											X	X																						WRITE 4 BYTES OF ZERO
		00		00	00		2		X				X											X	X																						
		00		00	00		1		X				X											X	X																						
		00		00	00		0		X				X											X	X																						
F	3	00	D	00	00				X		X	X			X																																WRITE 1 BYTE OF ZERO; CALL FOR IAM
F	4	IAM	→	00	00				X		X				X								X			X			X																		X = 36, WRITE 1 BYTE OF ZERO; GET IAM
F	5			IAM	IAM	X	36		X					X	X	X								X	X			X		X	X											X					WRITE INDEX ADDRESS MARK WITH
				FF_x	FF_x		35		X					X	X	X								X	X			X		X	X											X					PROPER MISSING CLOCKS FOLLOWED
				FF_x	FF_x		↓		X					X	X	X								X	X			X		X	X											X					BY 25 BYTES OF FILL
				FF_x	FF_x		12		X					X	X	X								X	X			X		X	X											X					
				FF_x	FF_x		11		X					X	X	X								X	X			X		X	X											X					
→ F	6	00		00	00	X	10		X				X				X							X	X				X	X	X											X				X	WRITE 4 BYTES OF ZERO
		00		00	00		9		X				X				X							X	X				X	X	X											X				X	
		00		00	00		8		X				X				X							X	X				X	X	X											X				X	
		00		00	00		7		X				X				X							X	X				X	X	X											X				X	
F	7	00	D →	00	00	X	6		X		X	X												X	X				X		X																WRITE 2 BYTES OF ZERO;
		IDAM	D →	00	00	X	5		X		X	X												X	X				X		X																GET IDAM
F	8	TRK		IDAM	IDAM	X	4		X		X	X		X		X		X						X	X																						WRITE HEADER - IDAM HAS MISSING
		0		TRK	TRK		3		X		X	X		X		X		X						X	X																						CLOCK BITS.
		SEC		0	0		2		X		X	X		X		X		X						X	X																						
		0		SEC	SEC		1		X		X	X		X		X		X						X	X																						
		0-1		0	0		0		X		X	X		X		X		X						X	X																						
F	9				CRC				X									X	X																												WRITE CRC
F	10				CRC				X									X	X																												WRITE CRC
F	11			FF_x	FF_x	W	N		X												X	X	X			X			X	X																	LOAD XCTR 38
				FF_x	FF_x		N-1		X												X	X	X			X			X	X																	WRITE FILL CHARACTERS FOR LENGTH OF
				FF_x	FF_x		↓		X												X	X	X			X			X	X																	FIELD SET BY WC
				FF_x	FF_x		1		X												X	X	X			X			X	X																	
				FF_x	FF_x		0		X												X	X	X			X			X	X																	
F	12			FF_x	FF_x	X	38		X															X	X			X		X	X		X										X					WRITE 27 BYTES OF FILL CHARACTERS
				FF_x	FF_x		37		X															X	X			X		X	X		X										X					THEN BACK TO STEP F6
				FF_x	FF_x		↓		X															X	X			X		X	X		X										X					
				FF_x	FF_x		12		X															X	X			X		X	X		X										X					
				FF_x	FF_x		11		X															X	X			X		X	X		X										X					
└→	TO		F6																																												
																																				X											
																																				X	ALL OTHER POSITIONS										NOTE: WHEN LAST HEADER HAS BEEN
																																				X											WRITTEN, WC CONTAINS GREATEST POSSIBLE
																																				↓											NUMBER. INDEX ARRIVES BEFORE FIL ENDS,
																																															STOPING THE OPERATION 2/26/76

COMPARE SECTOR

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCA2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
C	0	00		00									X				X						X						X																	X	SET UP
C	1	ID AM	D→	00				X			X	X																						X			X										CHECK FOR MISSING CLOCKS ; X= 4
C	2	TRK	D→	ID AM		X	4	X			X	X												X	X										X												COMPARE DISC VS HEADER IMAGE
		0	D→	TRK			3	X			X	X												X	X										X												IN MEMORY
		SEC	D→	0			2	X			X	X												X	X										X												STEP IF X=0
		0	D→	SEC			1	X			X	X												X	X										X												
		CRC	D→	0			0	X			X	X												X	X										X												
C	3	CRC	D	CRC				X				X																										X						X			CHECK CRC ; GET DATA MA LO FROM MEMORY
C	4	00		00									X				X				X		X					X	X		X														X		X= 13 ; GET MA HI
C	5	00				X	13																	X	X																						WAIT 14 BYTE TIMES
		00					12																	X	X																						
		00					↓																	X	X																						
		00					1																	X	X																						
		00					0																	X	X																						
C	6	DAM	D→			W	-1	X			X	X									X																X			X							CHECK FOR MISSING CLOCKS OF DAM
C	7	N	D→	DAM			-2	X			X	X									X																		X	X						X	COMPARE DAM(DDAM) VS MEMORY ; SHIFT DATA FIELDS
C	8	N-1	D→	N			-3	X			X	X									X	X																	X	X							
		N-2	D→	N-1			-4	X			X	X									X	X																	X	X							
		↓	D→	↓			↓	X			X	X									X	X																	X	X							
		1	D→	N-N			·	X			X	X									X	X																	X	X							
		0	D→	1			0	X			X	X									X	X																	X	X							
C	9	CRC		0				X																															X	X							LAST DATA BYTE
C	10	CRC						X																																X	X						TEST CRC
C	11																																														WAIT ONE BYTE
C	12																																			X											OPERATION OVER; NOT BUSY; INTERRUPT
																																				X											
																																				X											
																																				X											
																																				X	ALL OTHER POSITIONS										
																																				↓											

2/26/76

STEP

ROM & PIN

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON FCB1-1	WRITE ON FCB1-2	FORCE FILL FCA2-1	DIR TO DOR ENABLE FCB1-7	DMA ENABLE FCB2-8	CLR DIR, DOR FCB1-3	CSR OUT ON FCB2-4	CSR "I" BIT ON FCB2-5	CSR OUT ENABLE FCA1-7	LOAD CYC FCB3-2	CYC ON WRITE FCB3-1	CYC OUT ENABLE FCA1-6	DMA TO MEMORY (DIRECTION) FCA1-8	DEC WC ENABLE FCB2-3	STEP IF WC = 0 FCB3-3	LOAD XCTR FCA1-5	DEC XCTR FCA1-1	STEP IF XCTR EQUAL FCB3-4	XCTR 2^5 (32) FCA2-8	XCTR 2^4 (16) FCA2-7	XCTR 2^3 (8) FCA2-6	XCTR 2^2 (4) FCA2-5	XCTR 2^1 (2) FCA2-4	XCTR 2^0 (1) FCA2-3	STEP CMD FCA2-2	BRANCH TO 6 - NOT ZERO FCB1-5	BR 0 IF CLOCK ERROR FCB2-1	BR 0 IF COMPARISON ERROR FCB3-5	END FCB1-4	CHECK AM CLOCK FCB3-7	H CYC ERROR EN FCB2-2	D AM ERROR EN FCB3-8	D CLOCK ERROR EN FCB2-7	D CYC ERROR EN FCB2-6	FORMAT FLAG FCB1-8	WRITE FLAG FCB1-6	LOAD MA LO FUNCTION FCA1-4	LOAD MA HI FUNCTION FCA1-2	XFR MA FCA1-3	
S	0												X																			X															STEP DRIVE HEAD
S	1					W	N														X	X																									WAIT UNTIL WC=0
							N-1														X	X																									
							↓														X	X																									
							1														X	X																									
							0														X	X																									
S	2																																			X											END OPERATION; BUSY OFF; INTERRUPT
																																				X											
																																				X											
																																				X											
																																				X											
																																				↓ ALL OTHER POSITIONS											

2/26/76

TIME
(SETTLE)

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
ROM & PIN								FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
T	0																																														DO NOTHING
T	1					W	N														X	X																									WAIT UNTIL WC=0
							|													X	X																									
							↓														X	X																									
							1														X	X																									
							0														X	X																									
T	2																																			X											OPERATION ENDS; NOT BUSY; INTERRUPT
																																				X											
																																				X											
																																				X											
																																				X											
																																				↓ ALL OTHER POSITIONS											

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READ NEXT SECTOR

EVERYTHING READY; PROGRAM KNOWS WHERE DISK IS; TURN ON IN GAP JUST BEFORE SECTOR ID.

WC = DATA FIELD + HEADER

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA	
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3	
N	0	00		00									X				X			X			X				X			X																X	X=18
N	1	ID AM	D→	00		x	18	X			X	X								X	X			X													X										
N	2	TRK	D→	ID AM		x	17	X			X	X								X	X			X	X			X	X		X																	READ HEADER UNTIL X=13
		0	D→	TRK			16	X			X	X								X	X			X	X			X	X		X																	
		SEC	D→	0			15	X			X	X								X	X			X	X			X	X		X																	
		0	D→	SEC			14	X			X	X								X	X			X	X			X	X		X																	
		CRC1	D→	0			13	X			X	X								X	X			X	X			X	X		X																	
N	3	CRC2	D→	CRC1				X			X	X								X	X																	X									READ HEADER CRC
N	4			CRC2													X			X																											HEADER CRC 2 TO MEMORY
N	5						12																	X	X																						WAIT : PASS OVER GAP
							11																	X	X																						
							↓																	X	X																						
							1																	X	X																						
							0																	X	X																						
N	6	DAM	D→	CRC2				X			X	X								X	X																X			X							CHECK DAM CLOCK
N	7	1	D→	DAM		W		X			X	X								X	X	X																		X							
		2	D→	1				X			X	X								X	X	X																		X							
			D→				↓	X			X	X								X	X	X																		X							
		0	D→				1	X			X	X								X	X	X																		X							
		CRC1	D→	0			0	X			X	X								X	X	X																		X							
N	8	CRC2	D→	CRC1				X			X	X								X																				X	X						CRC1 TO MEMORY; CHECK CRC
N	9	CRC2		CRC2																X																											CRC2 TO MEMORY
N	10																																		|X|											OPERATION OVER; NOT BUSY; INTERRUPT
																																			|X|											
																																			|X|											
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																																			|X|											
																																			|X|											
																																			|↓ ALL OTHER POSITIONS|											

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NOP +RESERVED

COMMAND	STEP	DIR CONTENTS	DIR XFR TO DOR; DMA CYCLE	DOR CONTENTS	WRITTEN ON DISK	CONTROLLING COUNTER	COUNTER CONTENTS	READ ON	WRITE ON	FORCE FILL	DIR TO DOR ENABLE	DMA ENABLE	CLR DIR, DOR	CSR OUT ON	CSR "I" BIT ON	CSR OUT ENABLE	LOAD CYC	CYC ON WRITE	CYC OUT ENABLE	DMA TO MEMORY (DIRECTION)	DEC WC ENABLE	STEP IF WC = 0	LOAD XCTR	DEC XCTR	STEP IF XCTR EQUAL	XCTR 2^5 (32)	XCTR 2^4 (16)	XCTR 2^3 (8)	XCTR 2^2 (4)	XCTR 2^1 (2)	XCTR 2^0 (1)	STEP CMD	BRANCH TO 6 - NOT ZERO	BR 0 IF CLOCK ERROR	BR 0 IF COMPARISON ERROR	END	CHECK AM CLOCK	H CYC ERROR EN	D AM ERROR EN	D CLOCK ERROR EN	D CYC ERROR EN	FORMAT FLAG	WRITE FLAG	LOAD MA LO FUNCTION	LOAD MA HI FUNCTION	XFR MA
							ROM & PIN	FCB1-1	FCB1-2	FCA2-1	FCB1-7	FCB2-8	FCB1-3	FCB2-4	FCB2-5	FCA1-7	FCB3-2	FCB3-1	FCA1-6	FCA1-8	FCB2-3	FCB3-3	FCA1-5	FCA1-1	FCB3-4	FCA2-8	FCA2-7	FCA2-6	FCA2-5	FCA2-4	FCA2-3	FCA2-2	FCB1-5	FCB2-1	FCB3-5	FCB1-4	FCB3-7	FCB2-2	FCB3-8	FCB2-7	FCB2-6	FCB1-8	FCB1-6	FCA1-4	FCA1-2	FCA1-3
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NOP DOES NOT HAVE "END" PRESENT AT NOP-0, RESERVED OPERATIONS DO. NOP AND RESERVED OPERATIONS HAVE "END" PRESENT AT ALL OTHER STEPS

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